

## Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Schematics Page Index	1.0	07'06'22	36	ICH8-M( GND) 5/5	1.0	07'06'22
02	Block Diagram	1.0	07'06'22	37	SATA HDD/CD-ROM	1.0	07'06'22
03	Merom(HOST BUS) 1/3	1.0	07'06'22	38	EC+KBC	1.0	07'06'22
04	Merom(HOST BUS) 2/3	1.0	07'06'22	39	Flash ROM/XBUS	1.0	07'06'22
05	Merom(Power/Gnd) 3/3	1.0	07'06'22	40	Mini-PCIE Card	1.0	07'06'22
06	CLOCK GEN	1.0	07'06'22	41	Bluetooth/CAM/OIDE	1.0	07'06'22
07	Crestline (HOST) 1/7	1.0	07'06'22	42	EXPRESS	1.0	07'06'22
08	Crestline (DMI) 2/7	1.0	07'06'22	43	BTB to Audio/MDC	1.0	07'06'22
09	Crestline (GRAPHIC) 3/7	1.0	07'06'22	44	FAN/Thermal-Sensor	1.0	07'06'22
10	Crestline (DDRII) 4/7	1.0	07'06'22	45	PCI (PCI BUS)	1.0	07'06'22
11	Crestline (POWER,VCC) 5/7	1.0	07'06'22	46	PCI (i.LINK)	1.0	07'06'22
12	Crestline (VCC CORE) 6/7	1.0	07'06'22	47	PCI (SD/MS-DUO)	1.0	07'06'22
13	Crestline (VSS) 7/7	1.0	07'06'22	48	USB2.0	1.0	07'06'22
14	DDRII(SO-DIMM_0) 1/3	1.0	07'06'22	49	LAN (88E8036)	1.0	07'06'22
15	DDRII(SO-DIMM_1) 2/3	1.0	07'06'22	50	Power Design Diagram	1.0	07'06'22
16	DDRII(Termination) 3/3	1.0	07'06'22	51	DCIN&Charger	1.0	07'06'22
17	VGA(PCI-E)	1.0	07'06'22	52	SYS Power (+3_3V/+5V)	1.0	07'06'22
18	VGA(STRAP)	1.0	07'06'22	53	SYS Power(+1_5V/+1_05V)	1.0	07'06'22
19	VGA(GDDR)#	1.0	07'06'22	54	DDR2 Power(+1_8V/+0_9V)	1.0	07'06'22
20	VGA(MULTIUSE)	1.0	07'06'22	55	CPU_Vcore---ISL6262A	1.0	07'06'22
21	VGA(LVDS/VDAC )	1.0	07'06'22	56	Others power plane	1.0	07'06'22
22	VRAM(GDDR)# 1/2	1.0	07'06'22	57	OVP protection	1.0	07'06'22
23	VRAM(GDDR)# 2/2	1.0	07'06'22	58	VGA POWER(+1_1V/ +1_2V)	1.0	07'06'22
24	VGA(POWER) 1/3	1.0	07'06'22	59	GMCH power	1.0	07'06'22
25	VGA(POWER) 2/3	1.0	07'06'22	60	HOLE	1.0	07'06'22
26	VGA(POWER) 3/3	1.0	07'06'22	61	EC+KBC(3925)	1.0	07'06'22
27	VRAM(BYPASS) 1/2	1.0	07'06'22	62	HDMI	1.0	07'06'22
28	VRAM(BYPASS) 2/2	1.0	07'06'22	63	ROBSON B to B Connector.	1.0	07'06'22
29	TVIN and OUT/Semi-PnP#	1.0	07'06'22	64	LED/Touch/Lid	1.0	07'06'22
30	CRT	1.0	07'06'22	65	History ( 1 )	1.0	07'06'22
31	LVDS	1.0	07'06'22	66	History ( 2 )	1.0	07'06'22
32	ICH8-M( PCI/USB ) 1/5	1.0	07'06'22	67			
33	ICH8-M( LPC,IDE,SATA )2/5	1.0	07'06'22	68			
34	ICH8-M( GPIO) 3/5	1.0	07'06'22	69			
35	ICH8-M( POWER) 4/5	1.0	07'06'22	70			

## BOM configuration

SKU	Stuff	No stuff
NB8M-256MB-Samsung	NV_,NVNB8M_,NV128bit_,NV16M_,NVH/S_,NVQ/S_	NC_*,NVNB8P_,NV64bit_,NV8M_,NVQ_,NVH_
NB8M-256MB-Qimonda	NV_,NVNB8M_,NV128bit_,NV16M_,NVQ_,NVQ/S_	/NC_*,NVNB8P_,NV64bit_,NV8M_,NVH/S_,NVH_
NB8M-256MB-Hynix	NV_,NVNB8M_,NV128bit_,NV16M_,NVH/S_,NVH_	NC_*,NVNB8P_,NV64bit_,NV8M_,NVQ_,NVQ/S_
NB8M-128MB-Samsung	NV_,NVNB8M_,NV64bit_,NV16M_,NVH/S_,NVQ/S_	NC_*,NVNB8P_,NV128bit_,NV8M_,NVQ_,NVH_
NB8M-128MB-Qimonda	NV_,NVNB8M_,NV64bit_,NV16M_,NVQ_,NVQ/S_	NC_*,NVNB8P_,NV128bit_,NV8M_,NVH/S_,NVH_
NB8M-128MB-Hynix	NV_,NVNB8M_,NV64bit_,NV16M_,NVH/S_,NVH_	NC_*,NVNB8P_,NV128bit_,NV8M_,NVQ_,NVQ/S_
NB8M-64MB-Hynix	NV_,NVNB8M_,NV64bit_,NV8M_,NVH/S_,NVH_	NC_*,NVNB8P_,NV128bit_,NV16M_,NVQ/S_,NVQ_
NB8M-64MB-Samsung	NV_,NVNB8M_,NV64bit_,NV8M_,NVH/S_,NVQ/S_	NC_*,NVNB8P_,NV128bit_,NV16M_,NVQ_,NVH_
NB8P-256MB-Samsung	NV_,NVNB8P_,NV128bit_,NV16M_,NVH/S_,NVQ/S_	NC_*,NVNB8M_,NV64bit_,NV8M_,NVQ_,NVH_
NB8P-256MB-Qimonda	NV_,NVNB8P_,NV128bit_,NV16M_,NVQ_,NVQ/S_	NC_*,NVNB8M_,NV64bit_,NV8M_,NVH/S_,NVH_
NB8P-256MB-Hynix	NV_,NVNB8P_,NV128bit_,NV16M_,NVH/S_,NVH_	NC_*,NVNB8M_,NV64bit_,NV8M_,NVQ_,NVQ/S_
GM965/GL960	CA_	No CA_

Dropped the NB8P-SE/128MB and NB8P-SE/64M for MOR request

"no CA\_" means all of other prefix including the "NC\_" prefix.

Project Code &amp; Schematics Subject: MS91 Main Board

PCB P/N:

1P-0076100-8010(FUBAI)  
1P-0076500-8010(HANNSTAR)  
1P-0076200-8010(NAN YA)

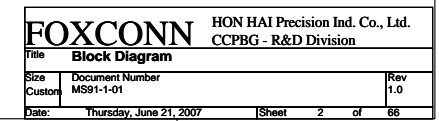
The "NC\_\*" include "NC\_CA\_"and "NC\_NV\*", the are prefix which comes from MS90 schematic,it means NC also, but if the component is needed again, "NC\_CA\_" is only for Low module only and "NC\_NV\*" only for HH/H/M module only.the rule is help to remind this.

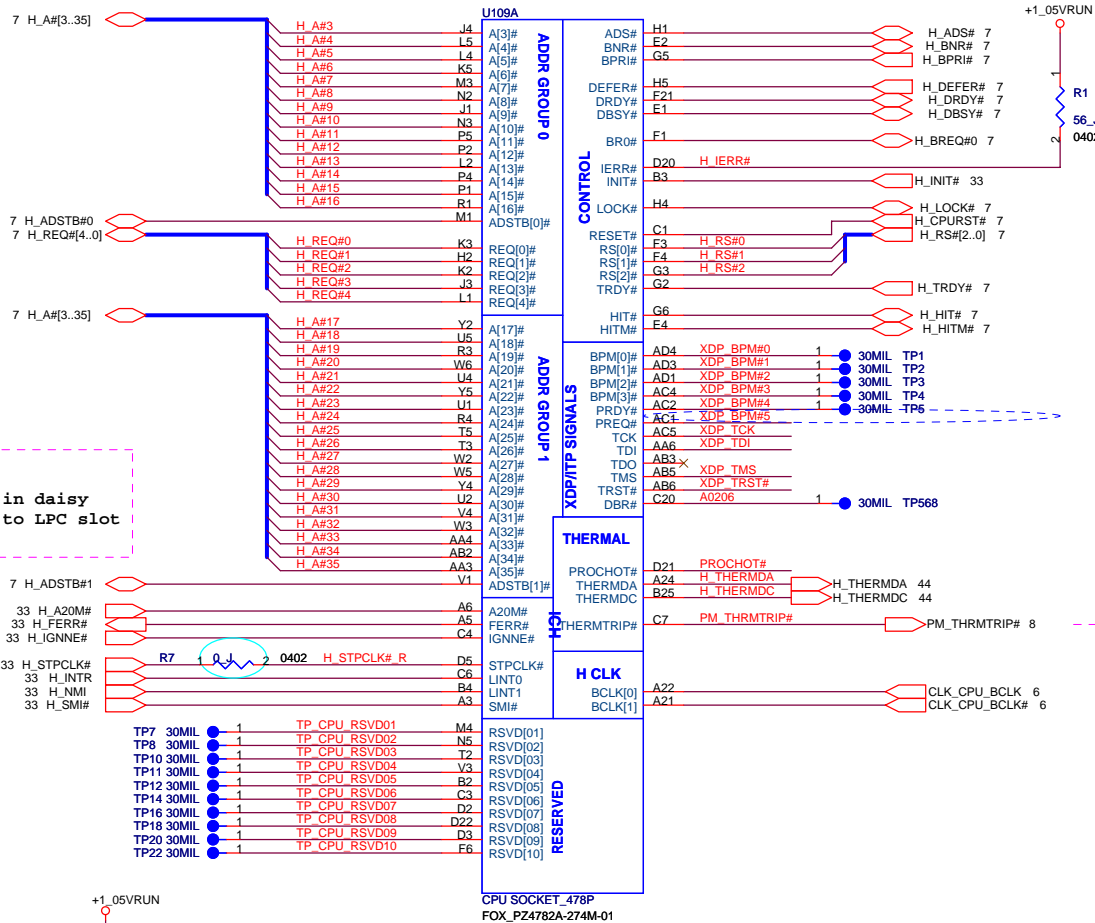
P. Leader	Check by	Design by

FOXCONN HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

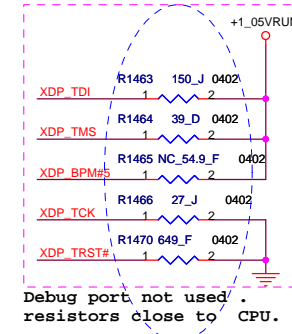
Title Index Page		
Size A3	Document Number MS91-1-01	Rev 1.0
Date: Thursday, June 21, 2007	Sheet 1	of 66

**WWW.AliSaler.Com**

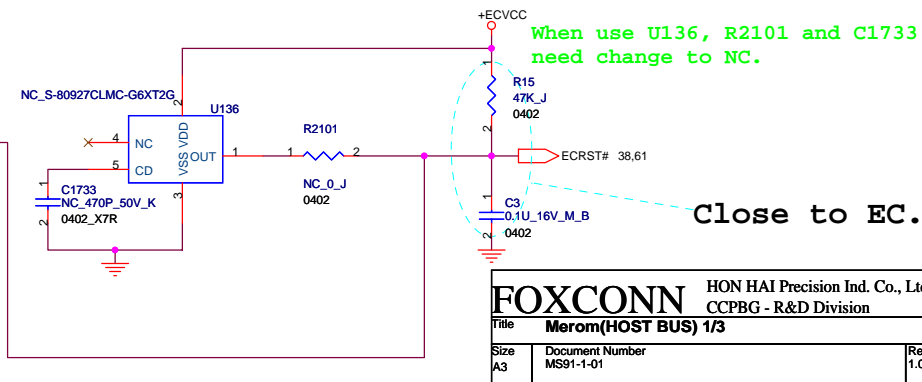
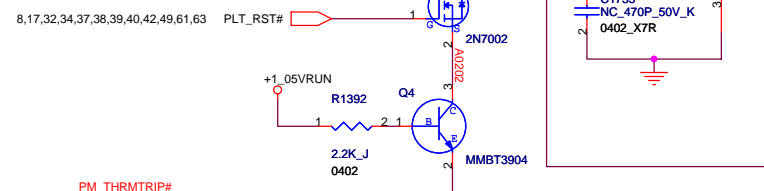
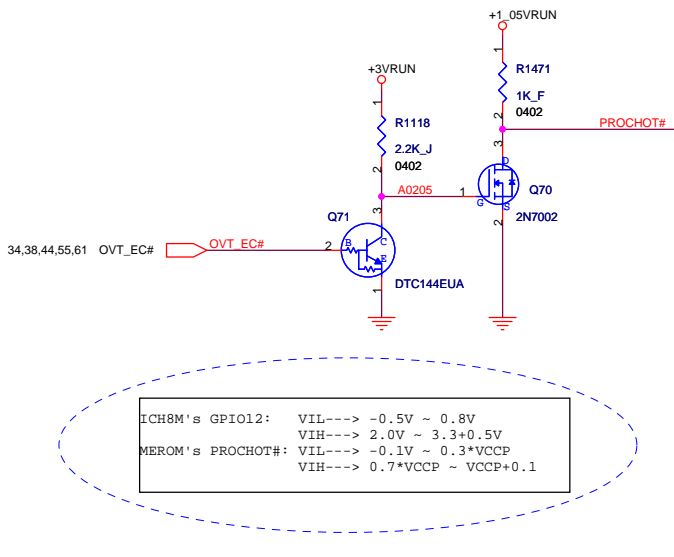




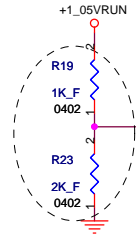
**Layout note:**  
no stub on H\_STPCLK TP.  
H\_STPCLK# to be routed in daisy chain fashion from ICH to LPC slot and then to CPU.



PM\_THRMTRIP# should connect to ICH8-M and GMCH without T-ing (No stub)



Place close to CPU



Place C817 close to the CPU\_TEST4 pin.  
Make sure CPU\_TEST4 routing is reference  
to GND and away from other noisy signals.

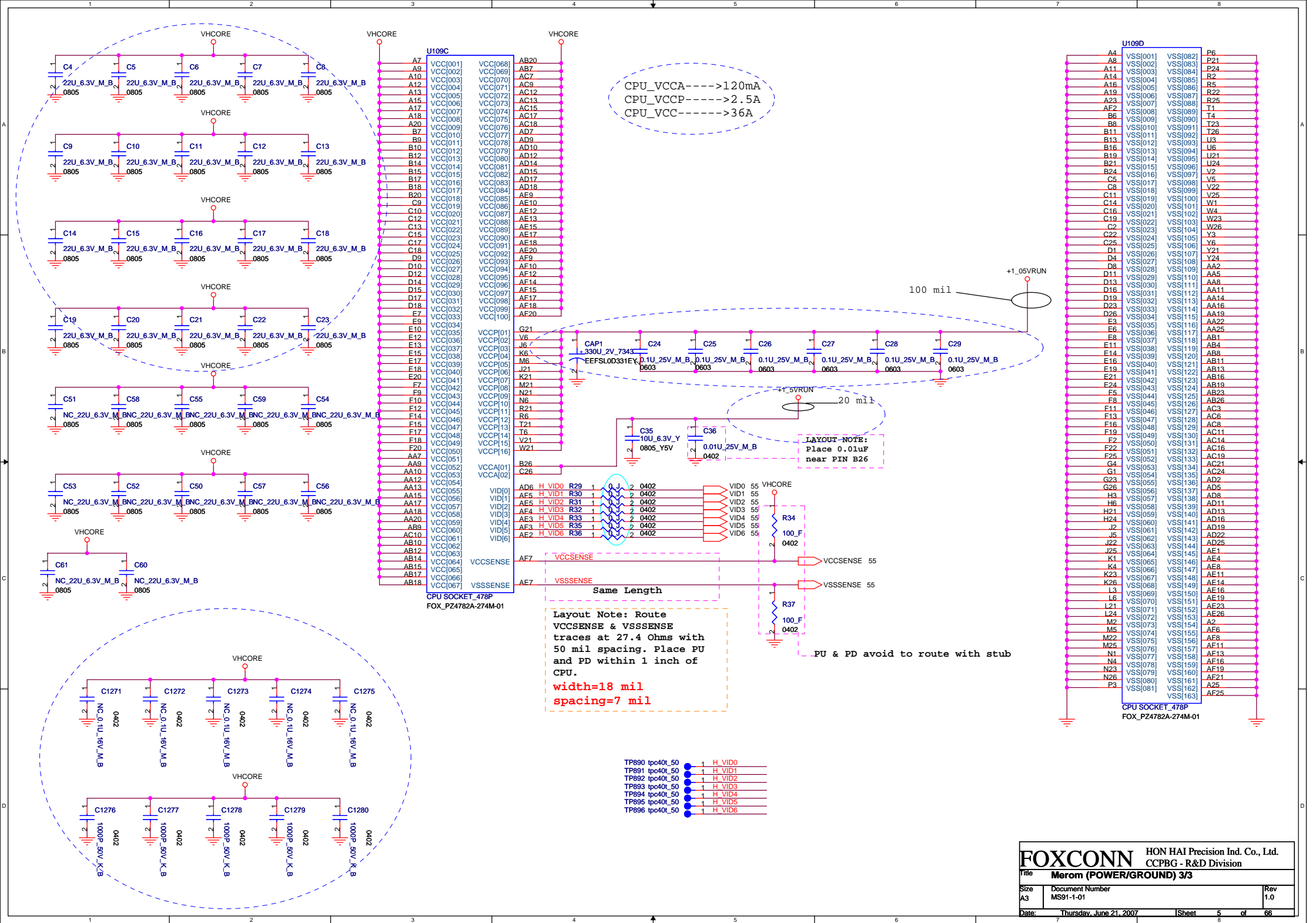
Layout Note:  
Zo=55 ohm, 0.5"  
max for GTLREF.

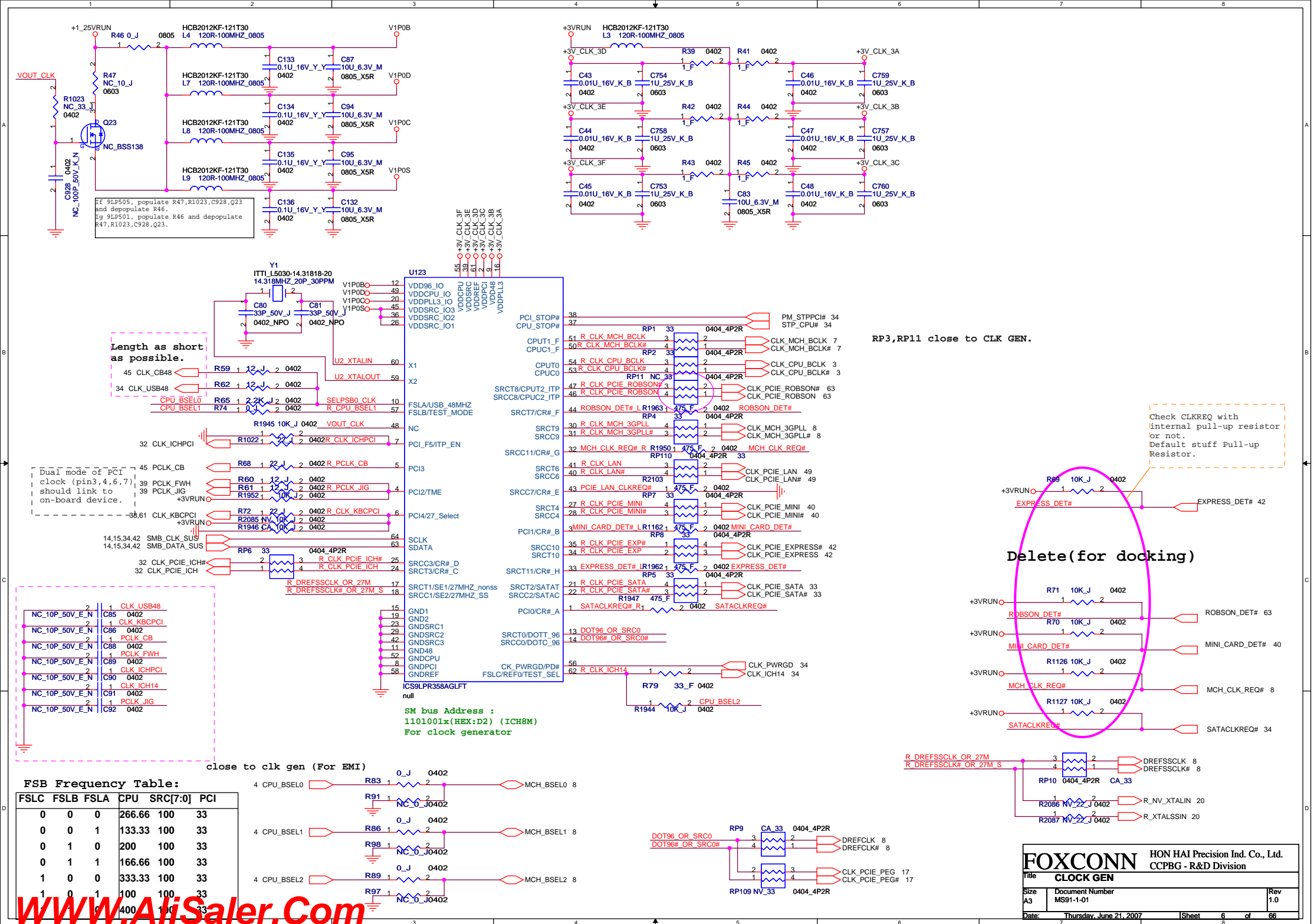
CPU SOCKET\_478P  
FOX\_P24782A-274M-01

Layout Note:  
Comp0,2 connect with Zo=27.4 ohm, make  
trace length shorter then 0.5".  
Comp1,3 connect with Zo=55 ohm, make  
trace length shorter then 0.5".

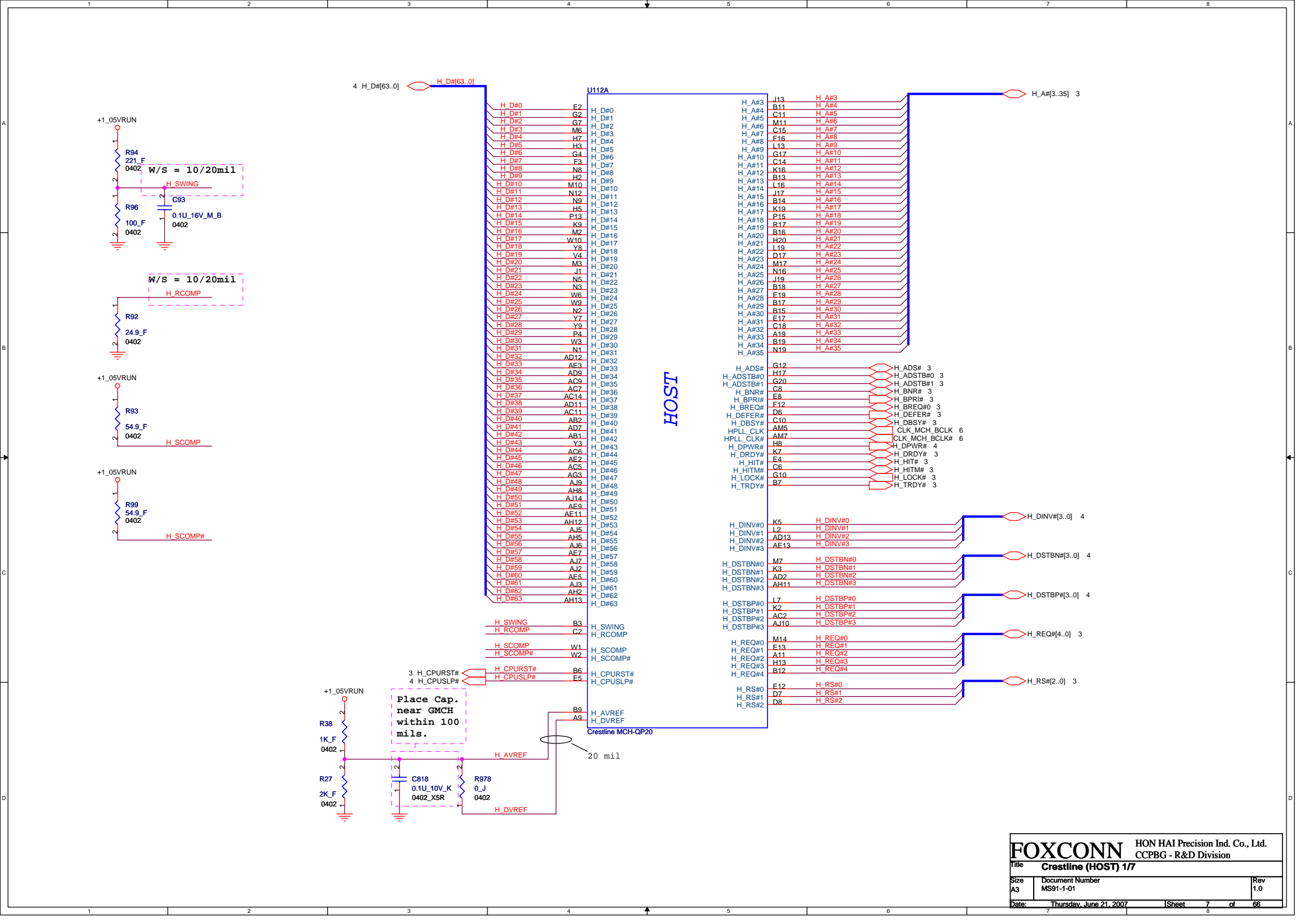
Layout:  
Connect test  
point with no  
stub

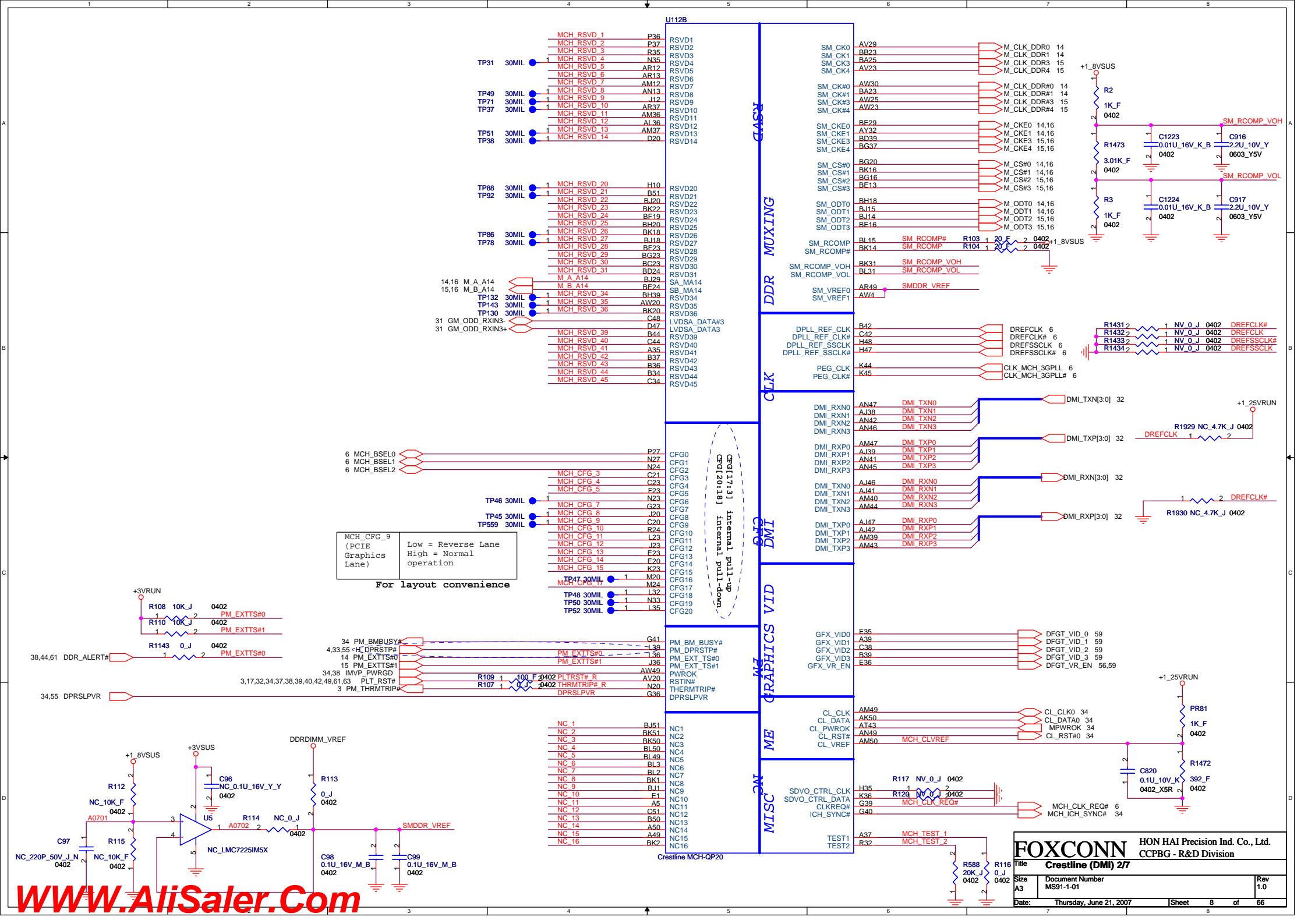
IMVP6 (ISL6262ACRZ-T)  
cpu PSI# <-> ISL6262ACRZ-T PSI#  
ISL6262ACRZ-T: VIHmin=0.315V  
VILmax=0.735V  
(ref. IMVP-6 NO:18904)



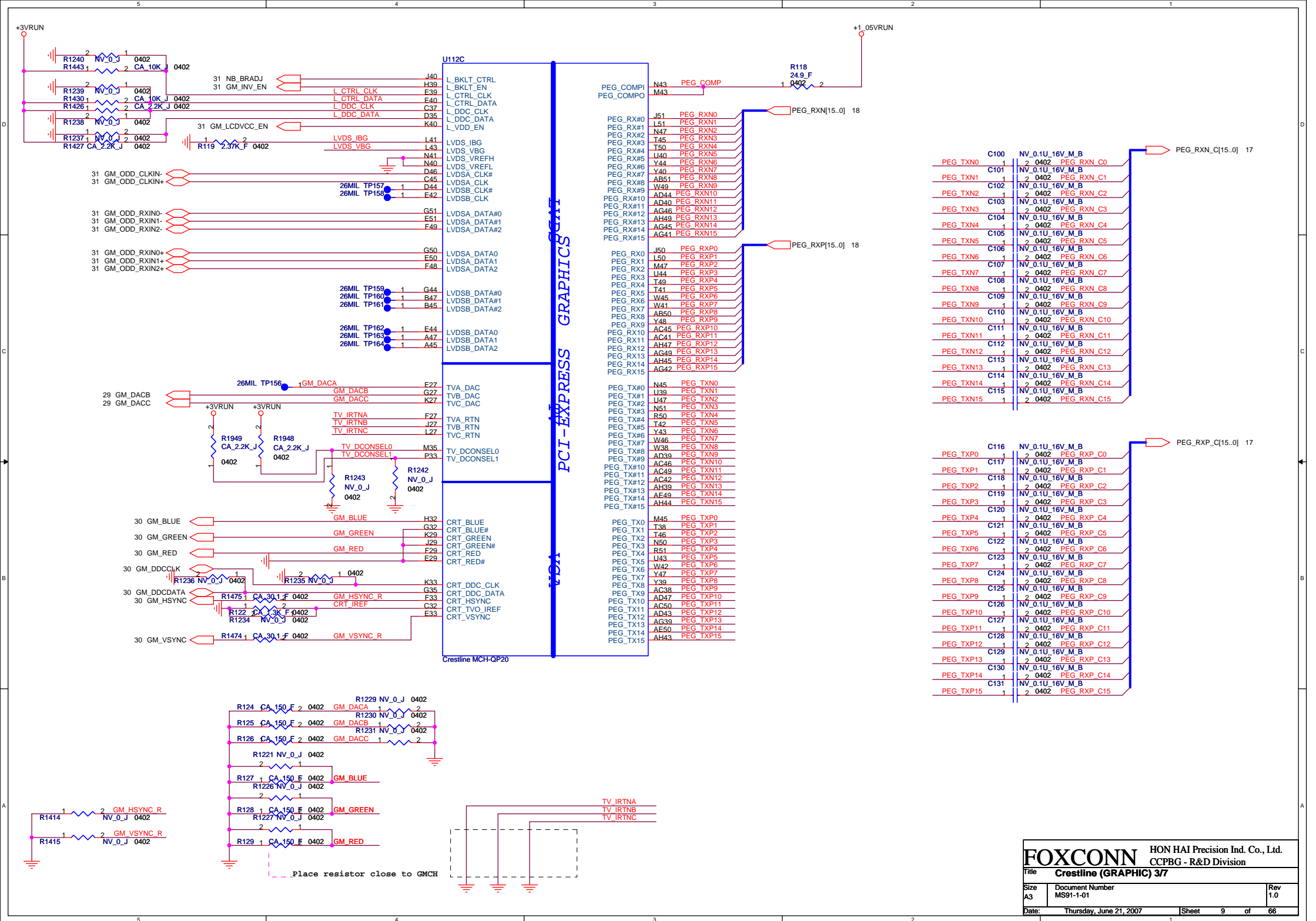




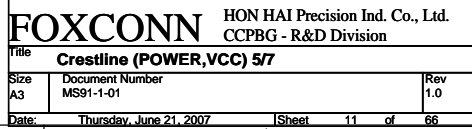




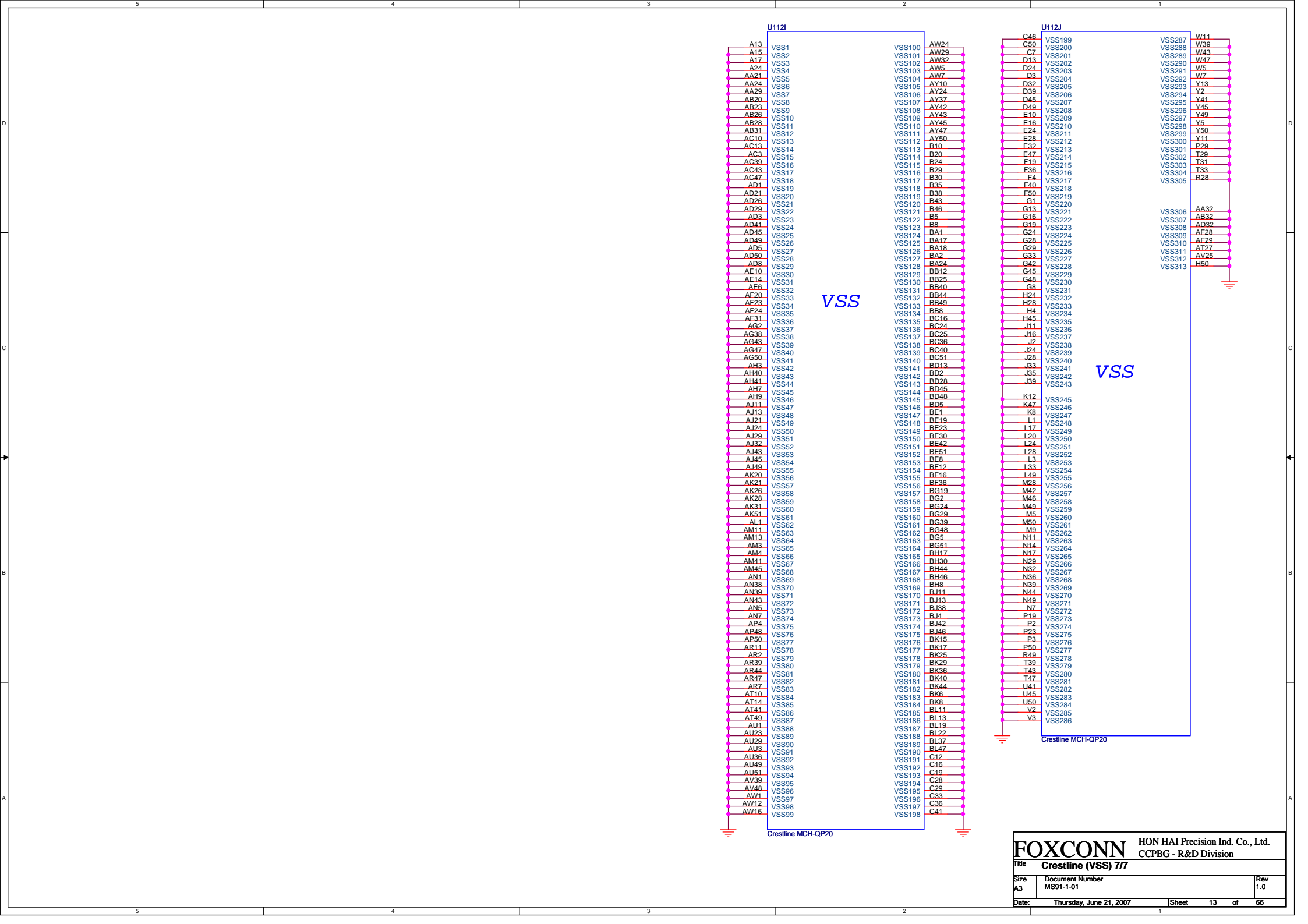








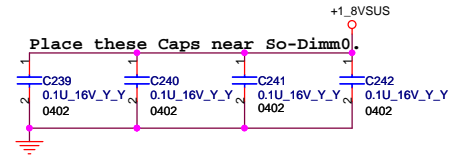
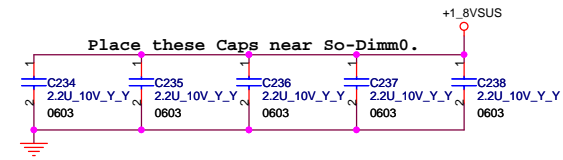
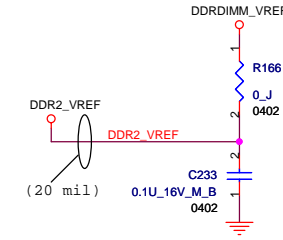
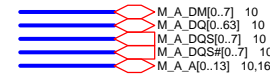






"Intel check list suggest a 330uF"

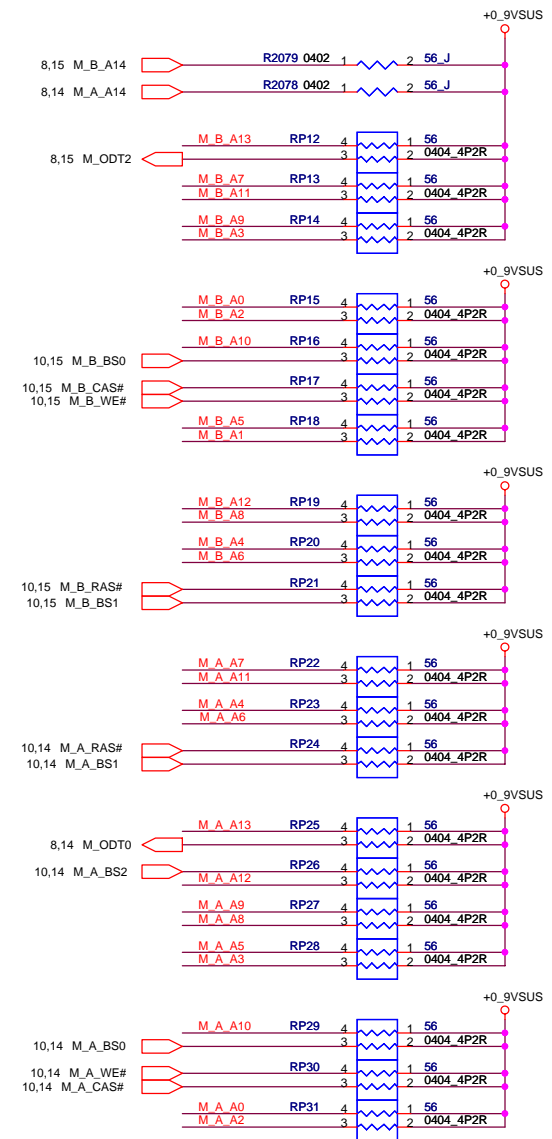
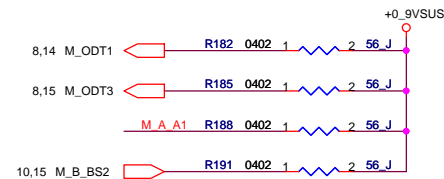
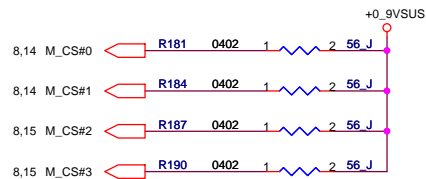
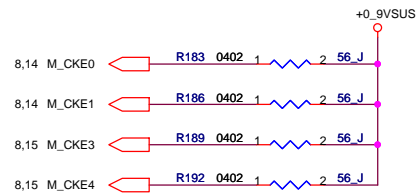
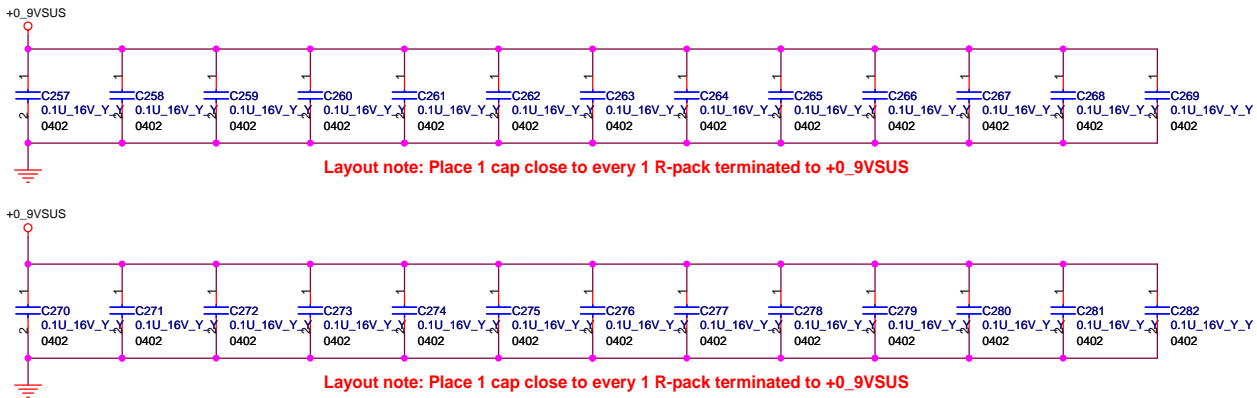
1.8V per DIMM=3.08A

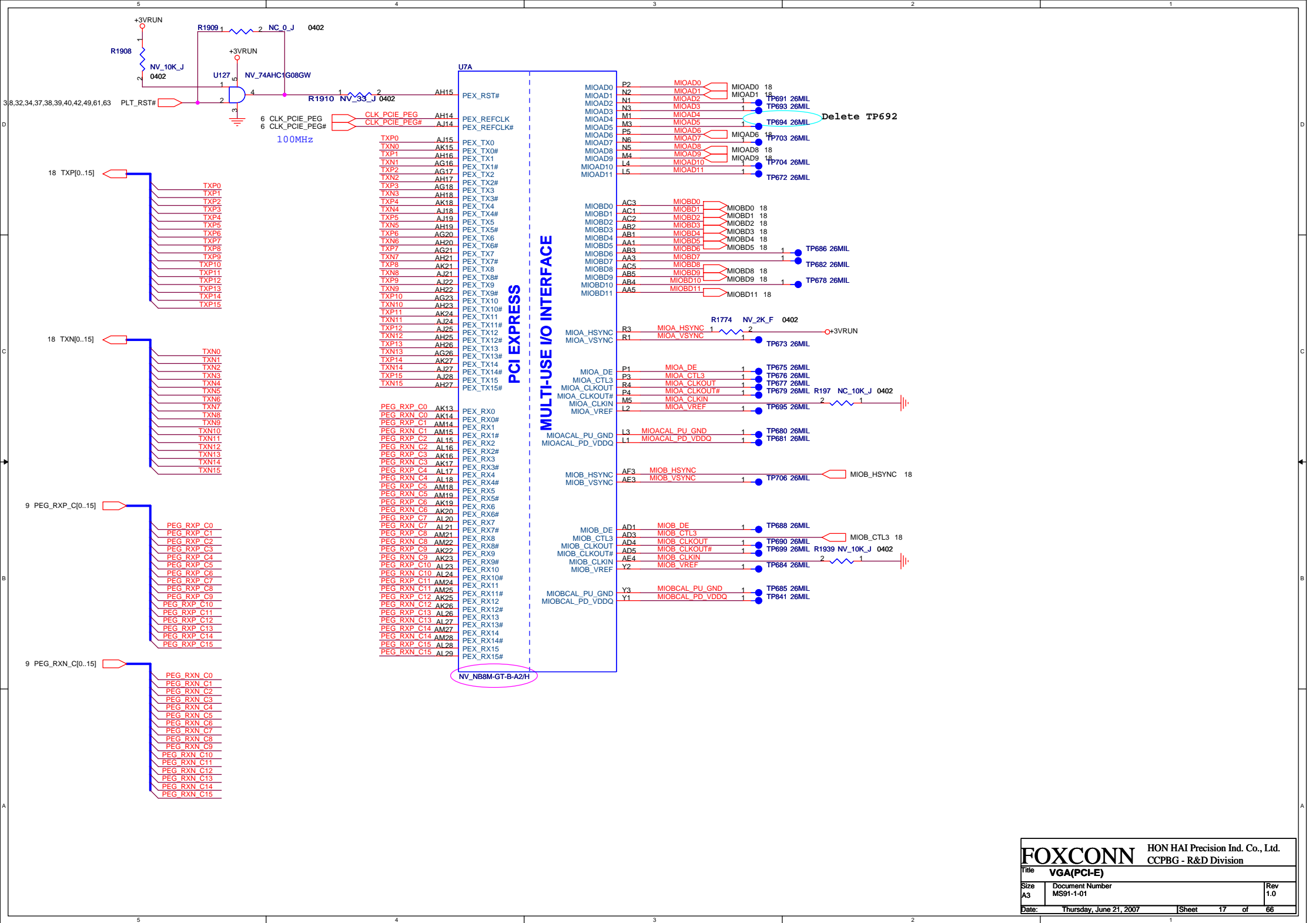


<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
Title		DDR(II)SO-DIMM_0	
Size	Document Number	Rev	
A3	MS91-1-01	1.0	
Date:	Thursday, June 21, 2007	Sheet	14 of 66



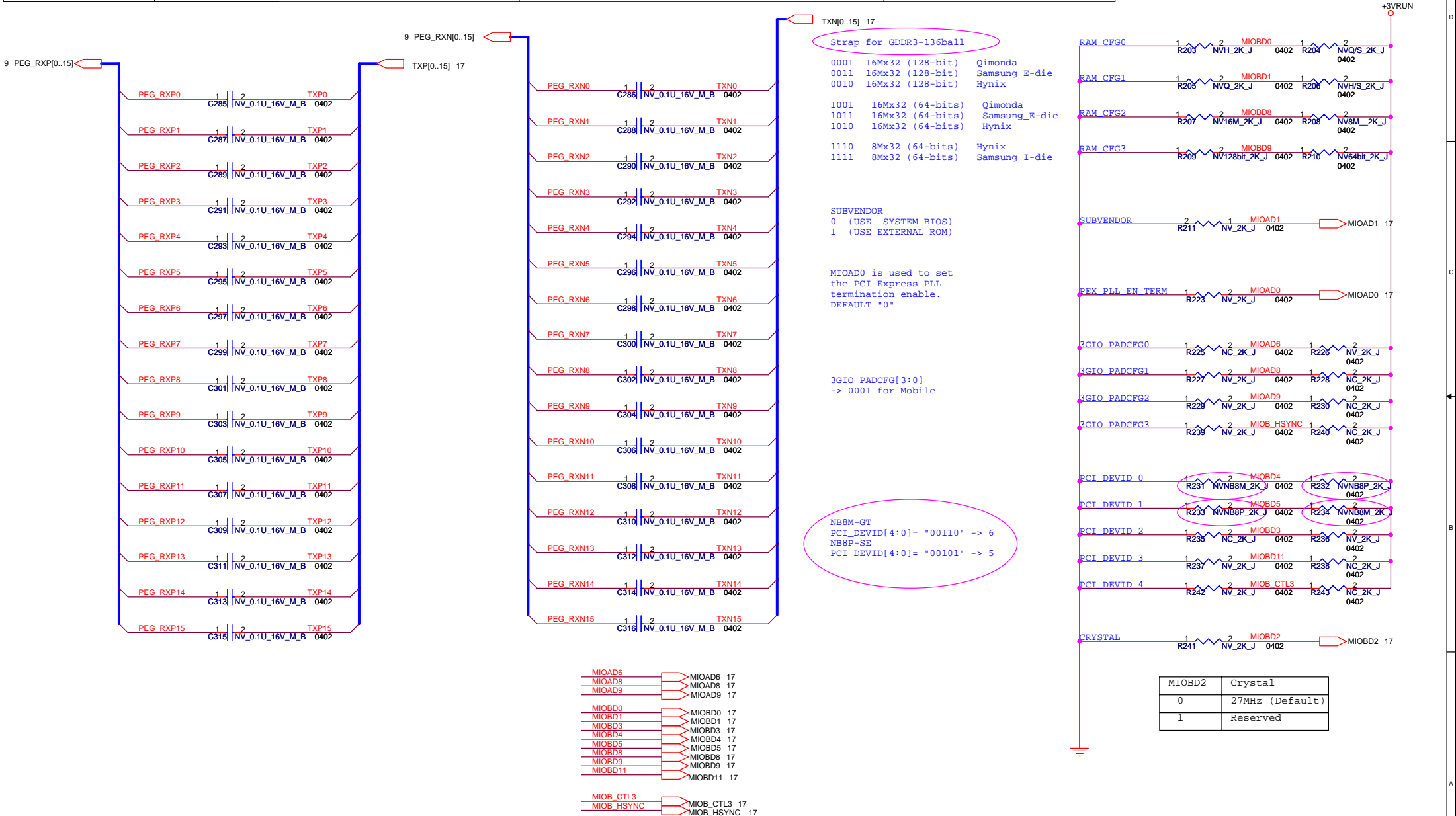




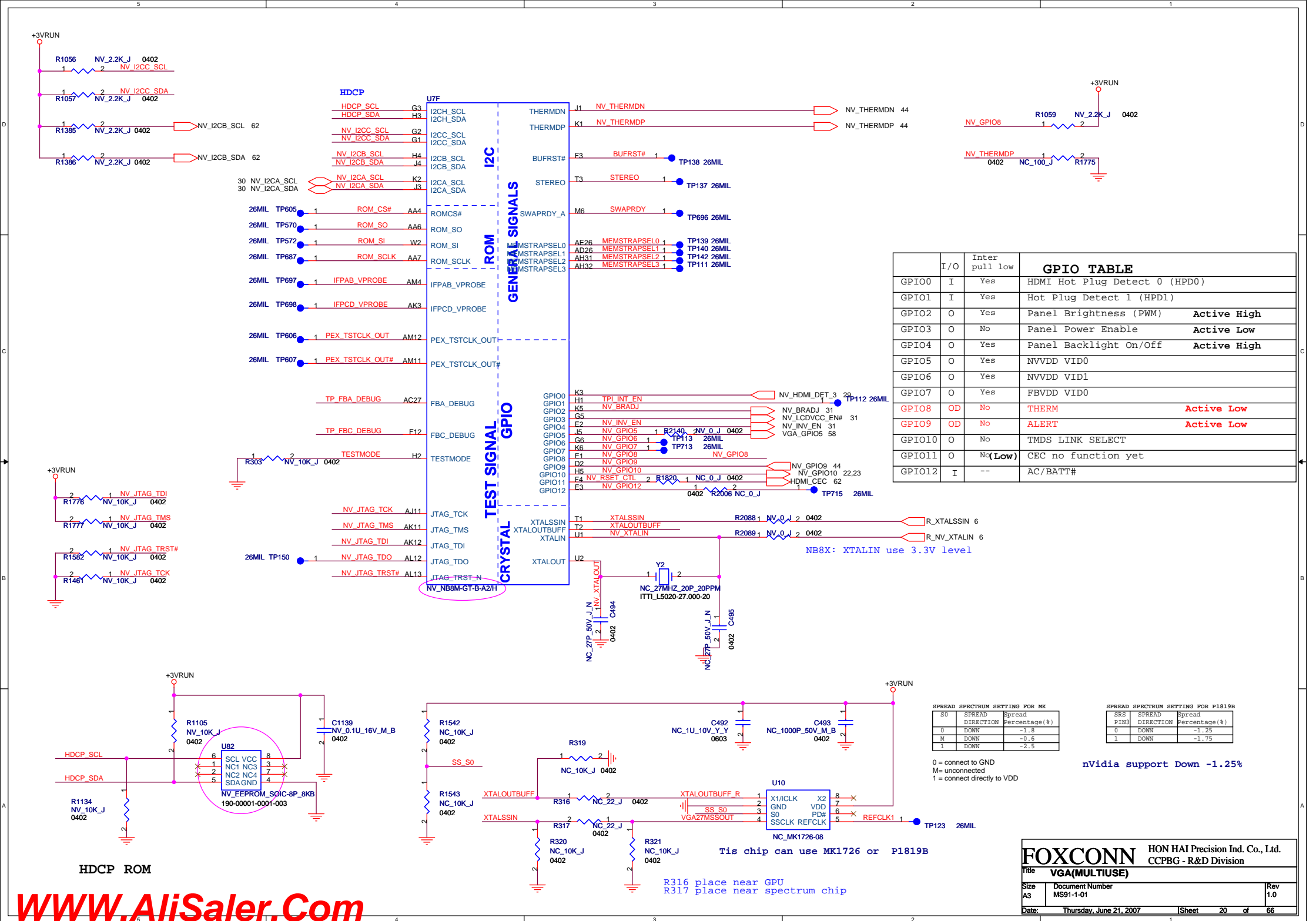


SKU	HH			H			M	
Vender	Hynix	Qimonda	Samsung	Qimonda	Samsung	Hynix	Samsung	Hynix
Vendor PN	HY5RS123235BFP-14	HYB18H512321BF-14	K4J52324QE-BC14	HYB18H512321BF-14	K4J52324QE-BC14	HY5RS123235BFP-14	K4J55323QI-BC14	HY5RS573225BFP-14
H.H PN	13-HY5RS12-3001	13-HYB18H5-3003	13-K4J5232-3001	13-HYB18H5-3003	13-K4J5232-3001	13-HY5RS12-3001	13-K4J5532-3003	13-HY5RS57-3003
Configuration	NB8X with 4pcs (16Mx32) GDDR3			NB8M-GT with 2pcs (16Mx32) GDDR3			NB8M-GT with 2pcs (8Mx32) GDDR3	
LOCATION	Stuff U11,U12,U13,U14			Stuff U11,U12; No stuff U13,U14			Stuff U11,U12; No stuff U13,U14	

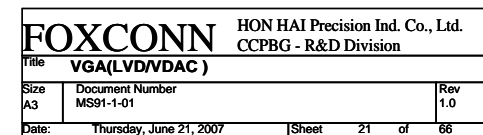
FAB: TV Mode Strap no use, remove.  
(MIOAD7, MIOAD10, MIOBD6)



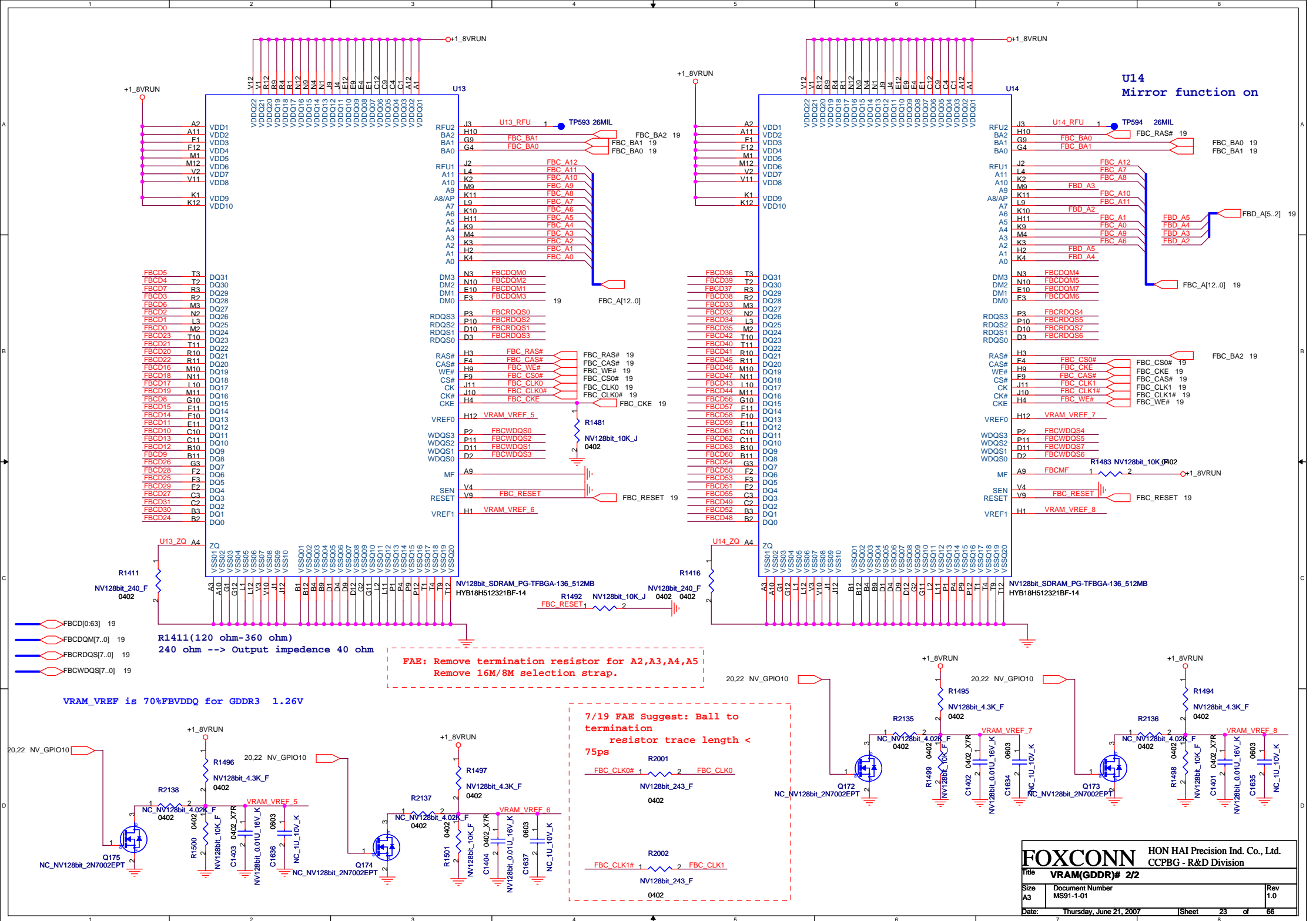


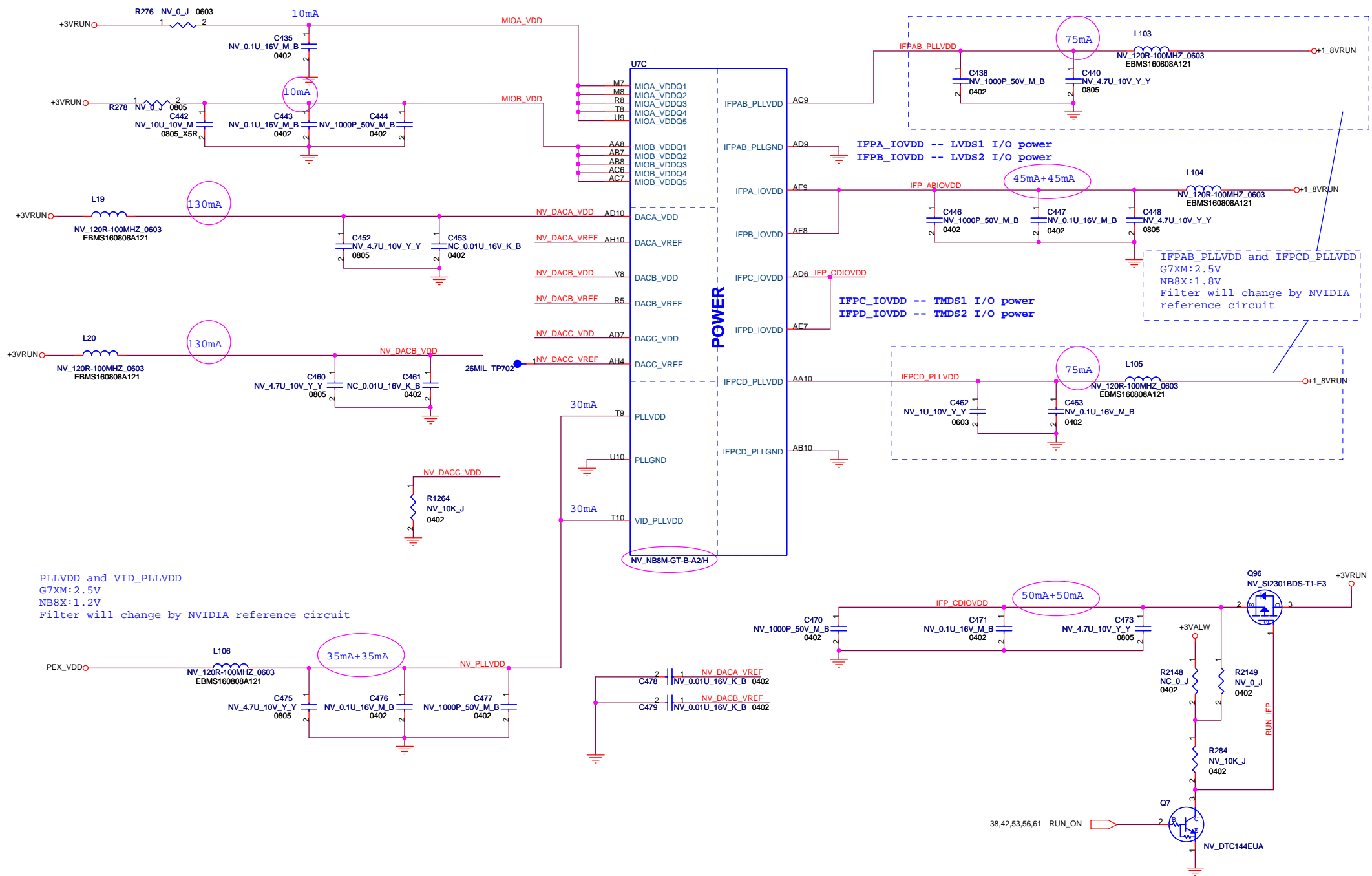








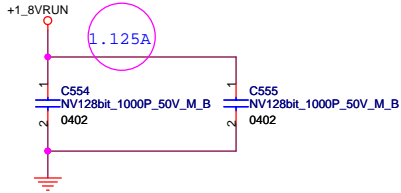
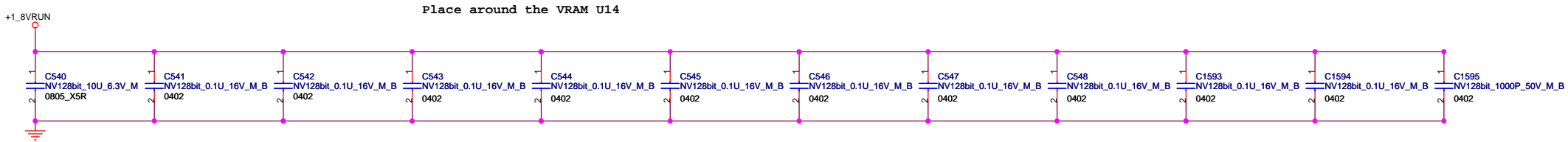
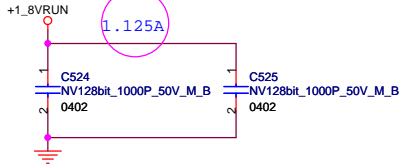
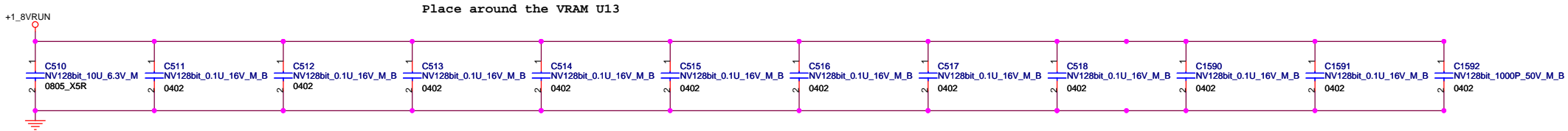


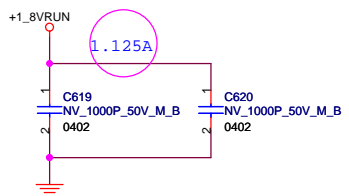
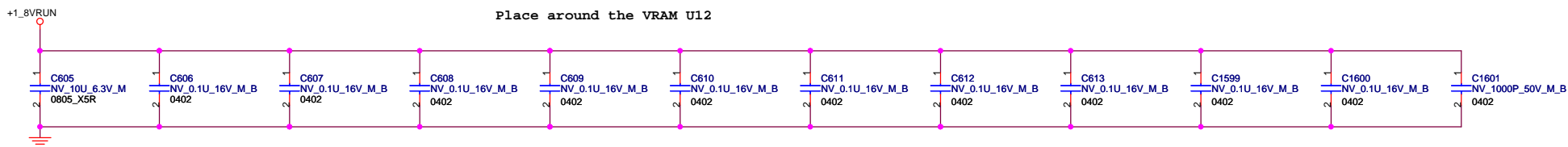
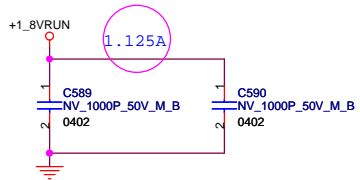
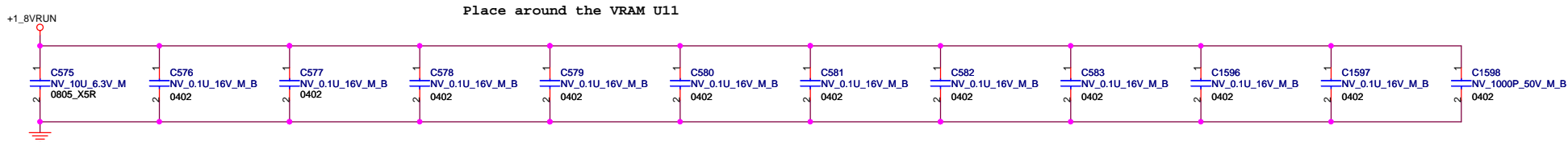




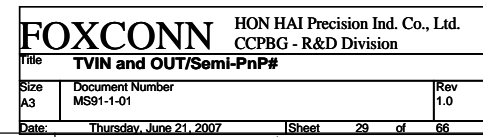








These component close to S-Video connector within 700 mil



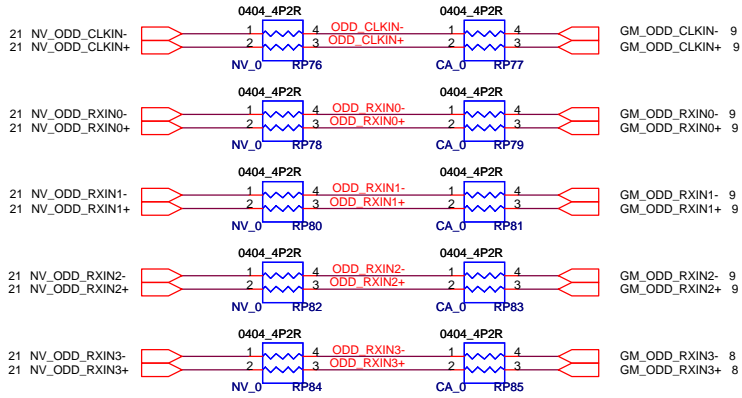


## LVDS

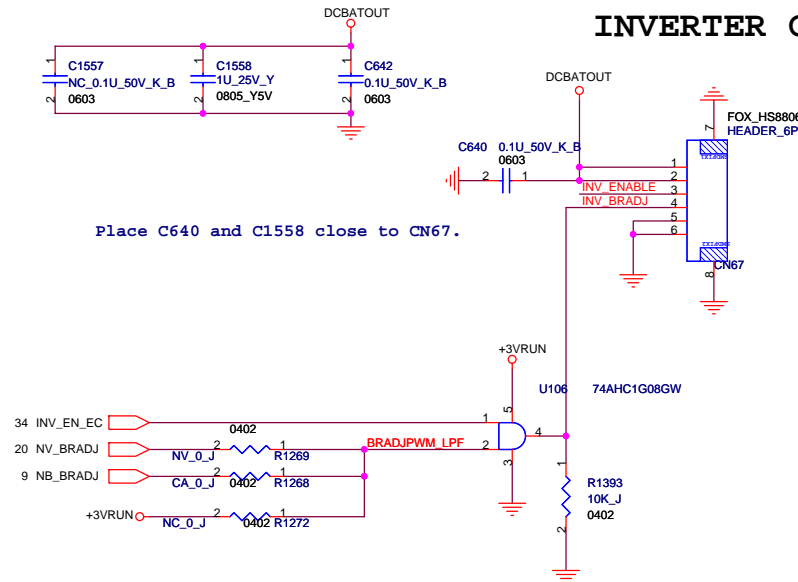
Group1, Group2 should be close

### Group1

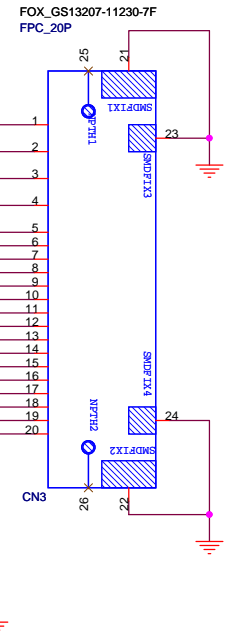
### Group2



## INVERTER CONN.

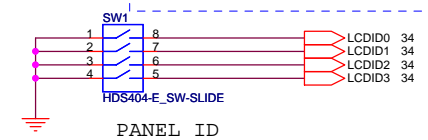


Place C640 and C1558 close to CN67.



## LVDS CONNECTOR

EVT use 30pin  
DVT modify to 20pin



Type	WXGA	WXGA	WXGA	WXGA
Size	15.4"W	15.4"W	15.4"W	15.4"W
Vender	Samsung (2 lamp)	CPT (1 lamp)	AUO (2 lamp)	AUO (1 lamp)
Device Name	LTN154XB-L01	CLAA154WA05AN	B154EW07	QD15TL07
Panel ID [2_0]	001	101	010	100

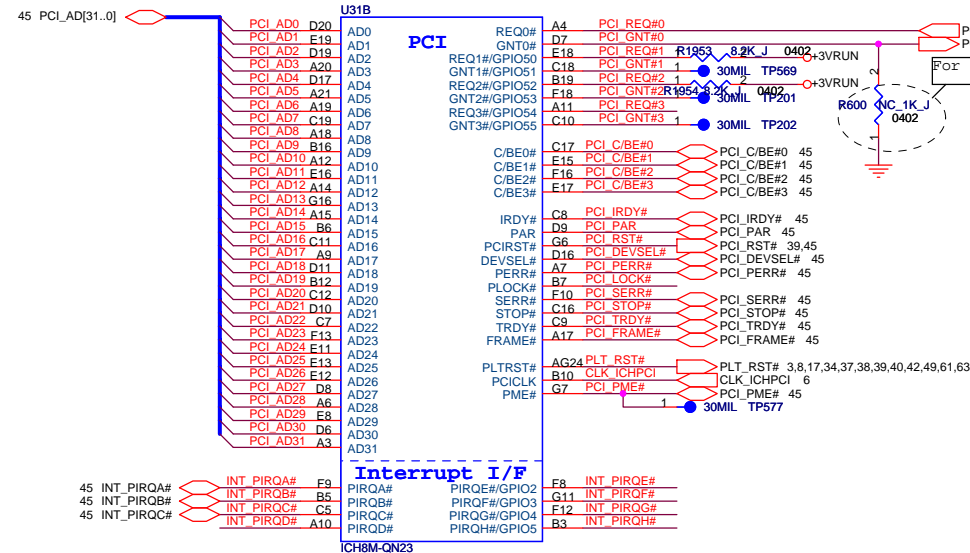
LCDID3 is for InstantOn switch  
Enable: 0  
Disable: 1

FOXCONN		HON HAI Precision Ind. Co., Ltd.	
Title		CCPBG - R&D Division	
Size	Document Number	Rev	
A3	MS91-1-01	1.0	
Date:	Thursday, June 21, 2007	Sheet	31 of 66

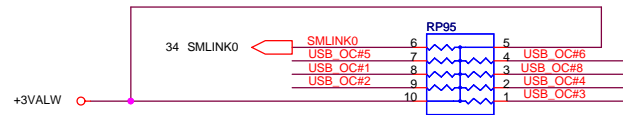
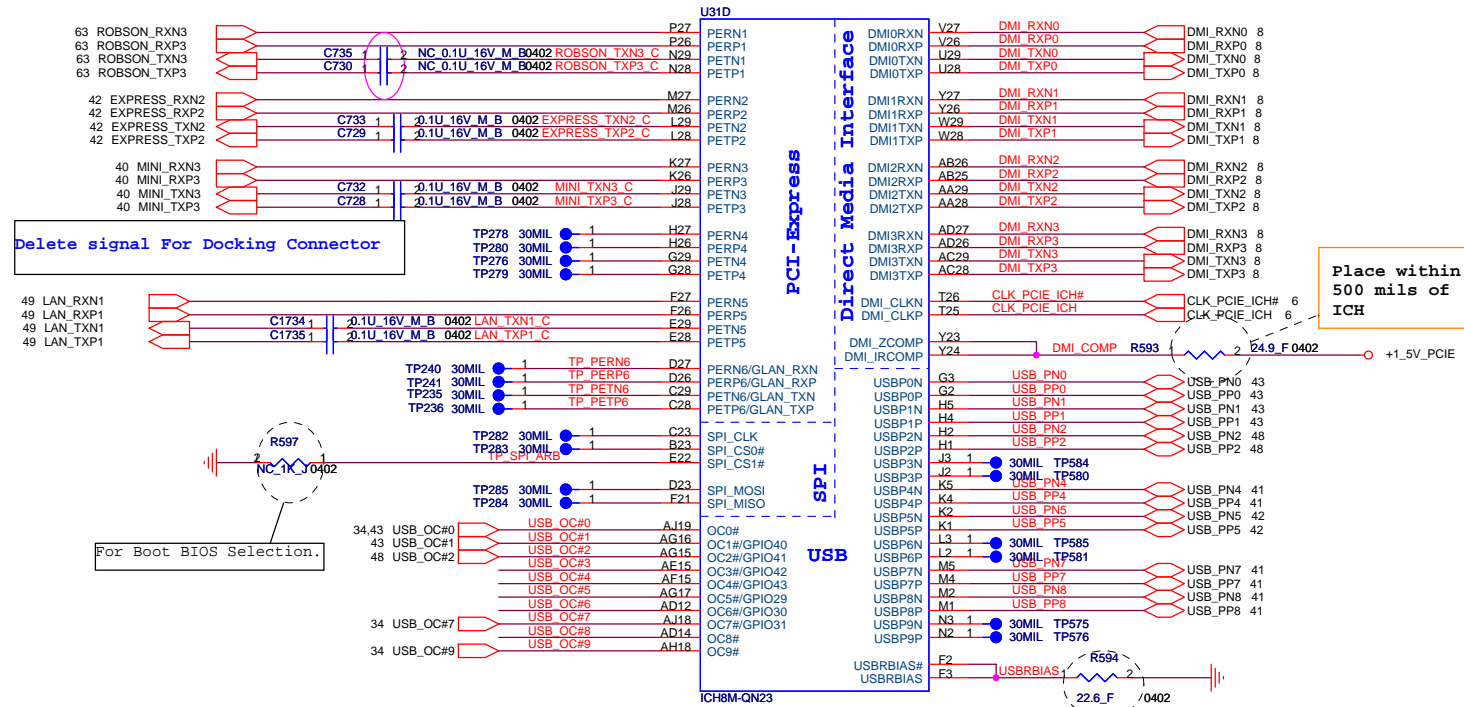
R459 close to R458.

DISCHARGE  
The R461 will consume about  
0.054 Watt (3.3x3.3/200 =  
0.054W). We changed resistor  
to 0603 size (1/8 Watt)

## PCI Pullups

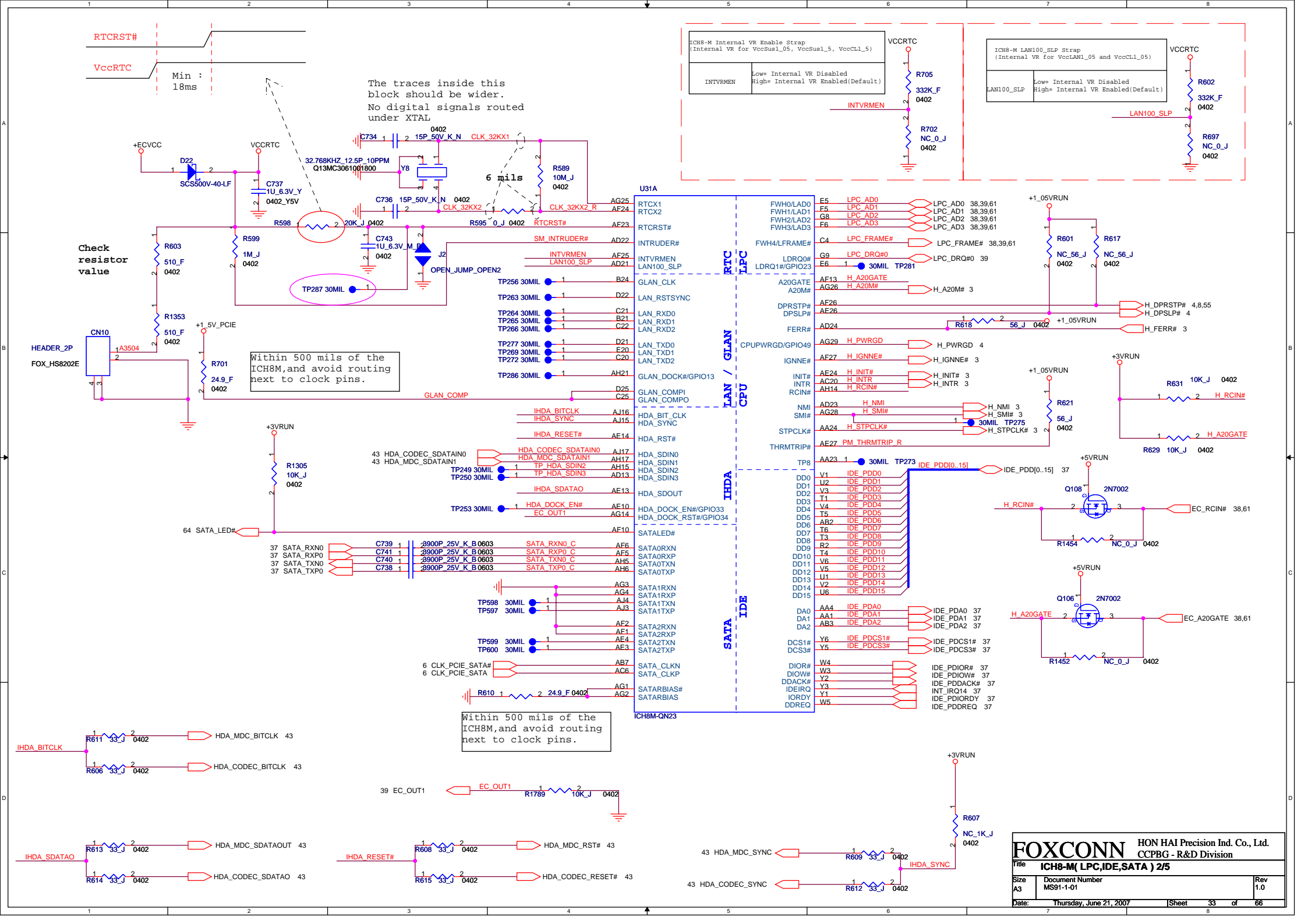


	GNT0#	SPI_CS1#
LPC(Default)	Hi	Hi
PCI	Hi	LOW
SPI	LOW	Hi

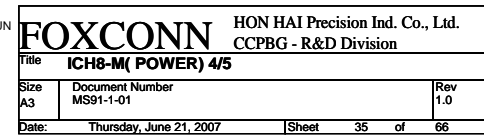


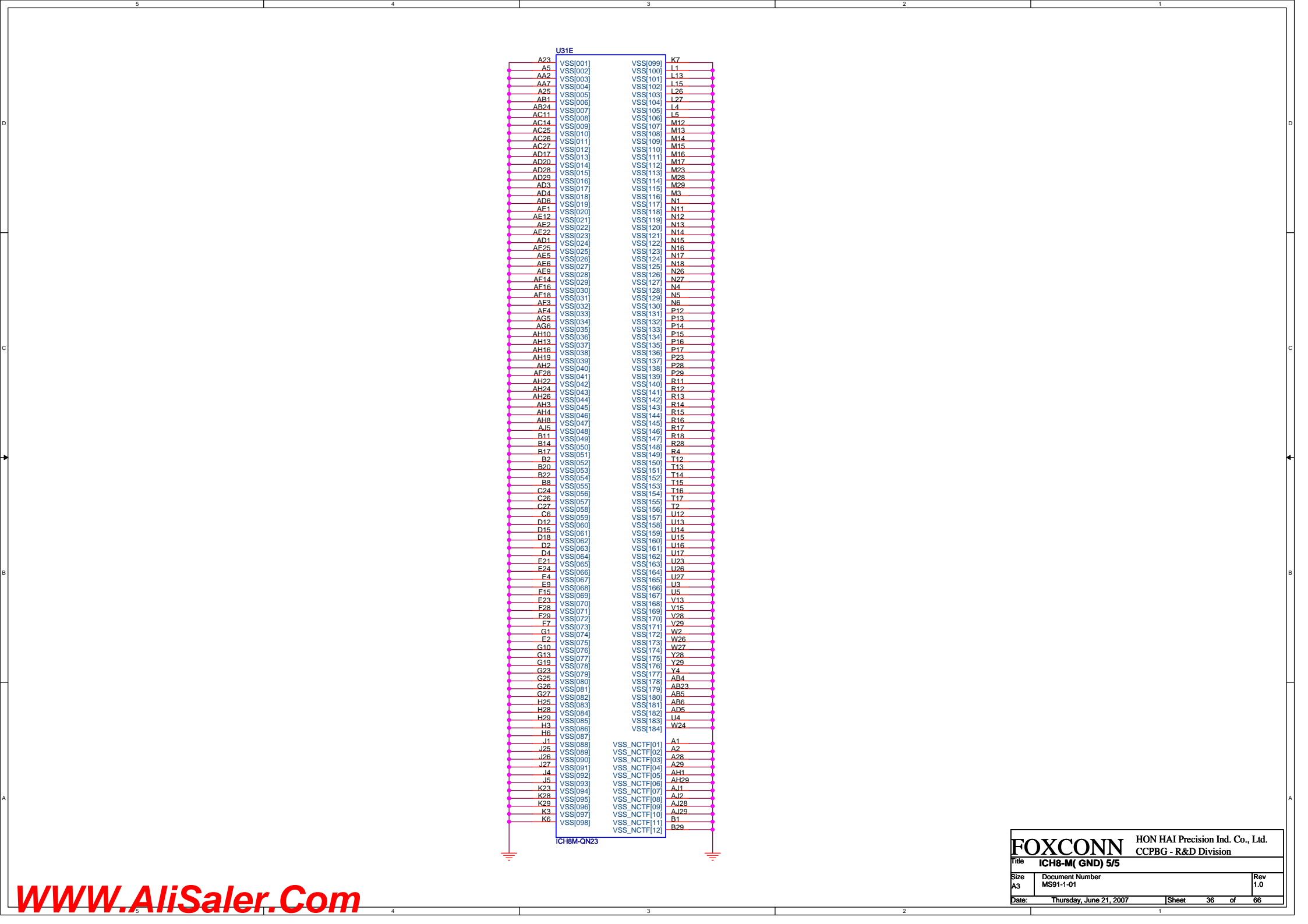
Place within 500 mils of  
ICH and don't routing next  
to high speed signals

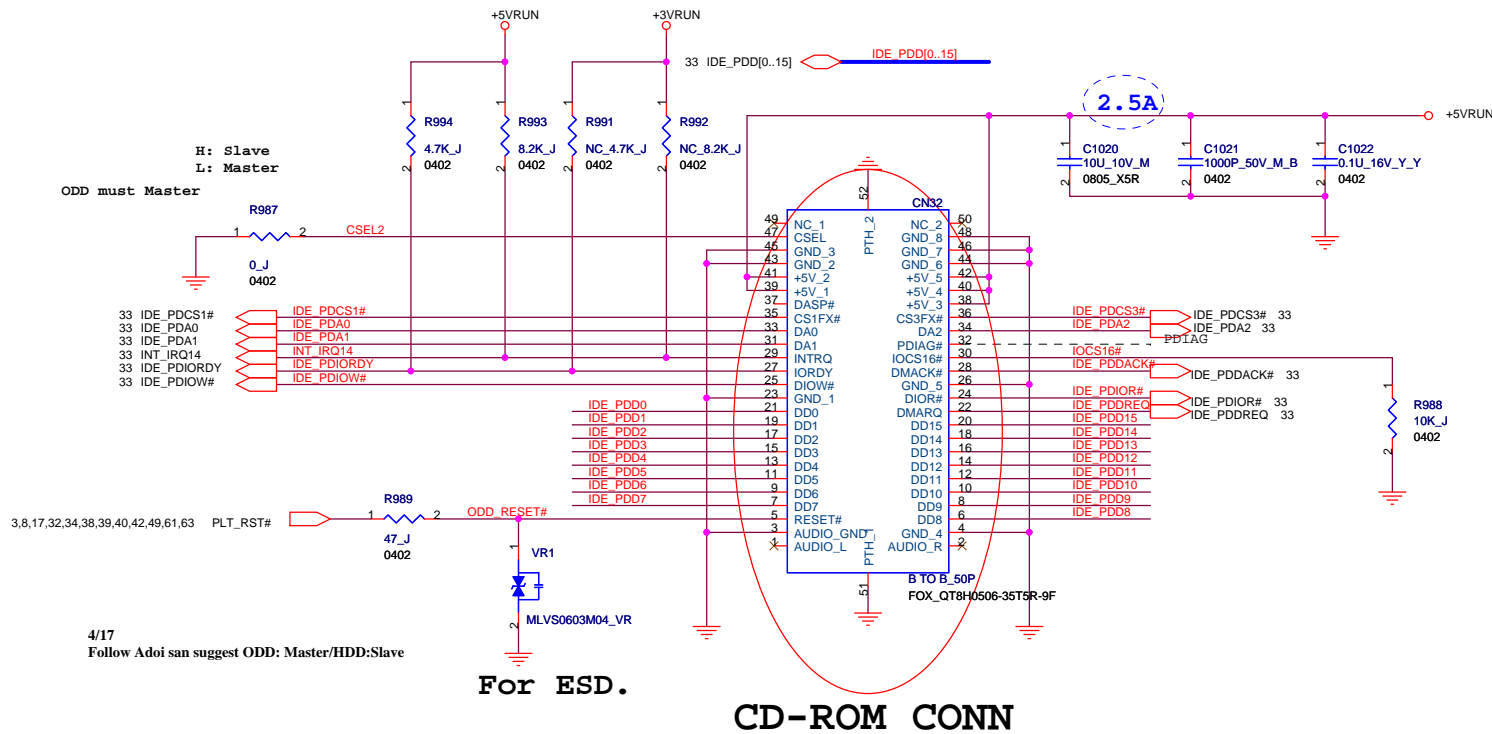
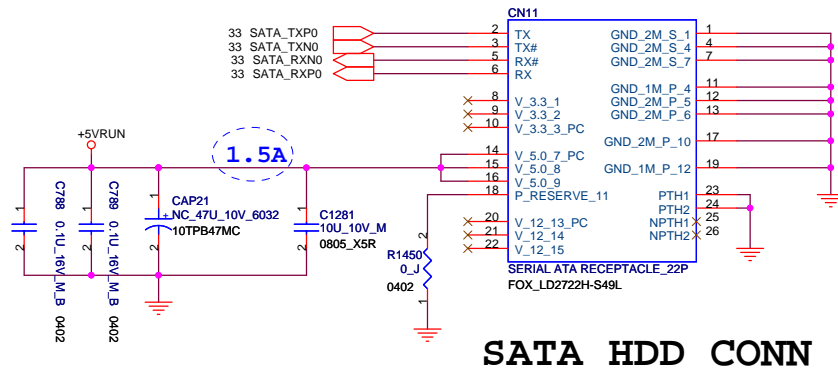




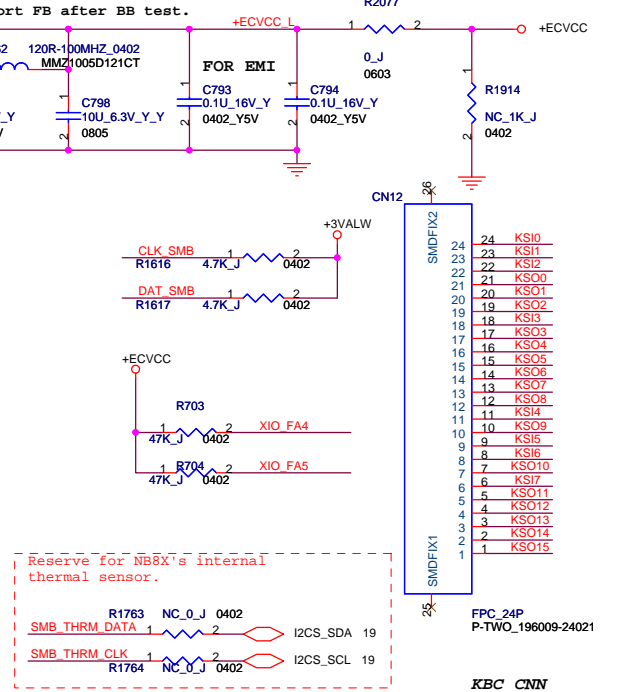
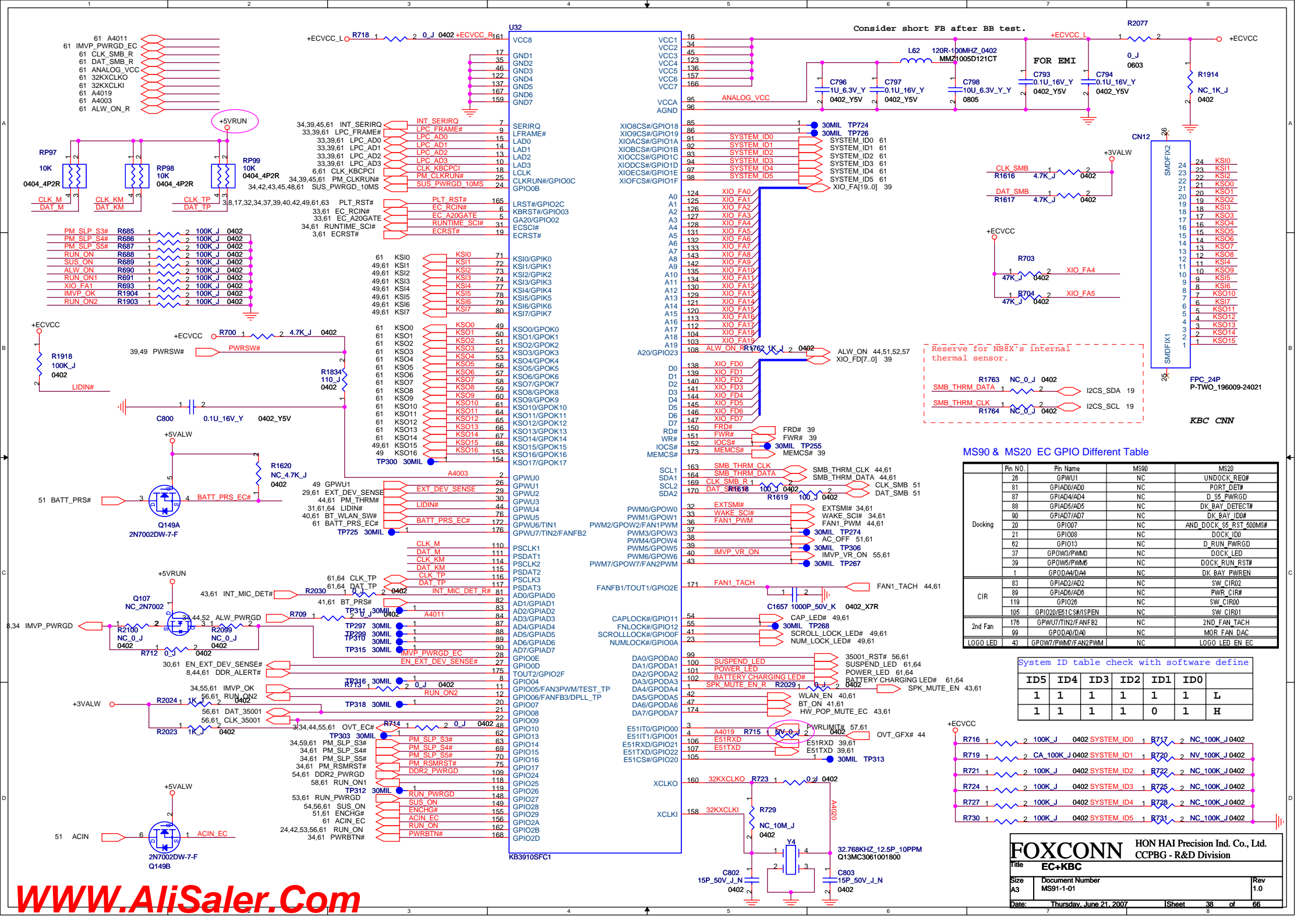










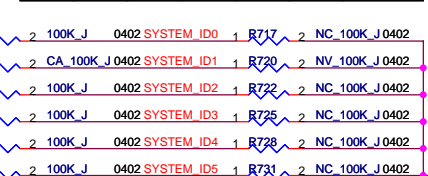


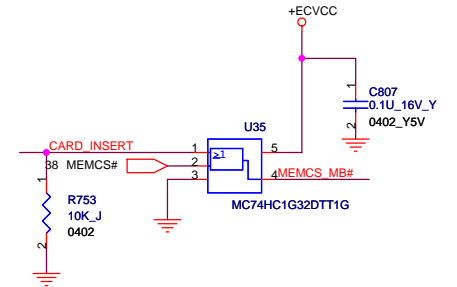
MS90 & MS20 EC GPIO Different Table

Pin NO.	Pin Name	MS90	MS20
26	GPWU1	NC	UNDOCK REQ#
81	GPWU1	NC	PORT_DET#
87	GPWU1	NC	D_S5_PWRGD
88	GPWU1	NC	DK_BAY_DETECT#
90	GPWU1	NC	DK_BAY_IDO#
20	GPWU1	NC	AND_DOCK_S5_RST_600MS#
21	GPWU1	NC	DOCK_IDO
62	GPWU1	NC	D_RUN_PWRGD
37	GPWU1	NC	DOCK_LED
39	GPWU1	NC	DOCK_RUN_RST#
1	GPWU1	NC	DK_BAY_PWREN
83	GPWU1	NC	SW_CIR02
89	GPWU1	NC	PWR_CIR0
119	GPWU1	NC	SW_CIR00
105	GPWU1	NC	SW_CIR01
176	GPWU1	NC	2ND_FAN_TACH
99	GPWU1	NC	MOR_FAN_DAC
43	GPWU1	NC	LOGO_LED_EN_EC

System ID table check with software define

ID5	ID4	ID3	ID2	ID1	ID0
1	1	1	1	1	L
1	1	1	1	0	H



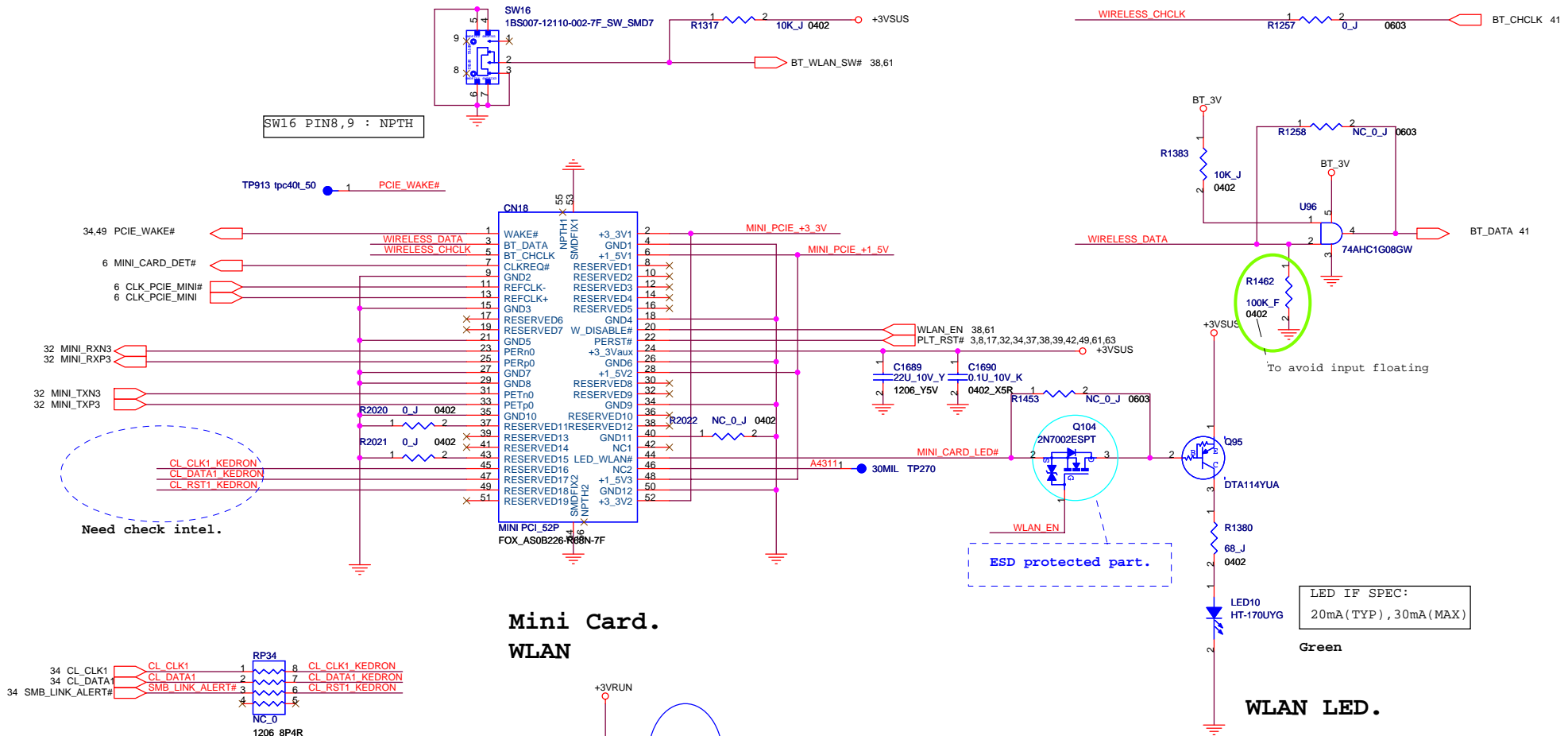


Pin connection diagram for CN15 connector. The diagram shows a 34-pin connector with pins numbered 1 to 34. Pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, 33, and 34 are connected to various signals. Pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, and 32 are connected to ground. The signals are: +ECVCC (pin 1), LPC\_AD1 (pin 3), LPC\_AD3 (pin 5), LPC\_DRQ#0 (pin 7), PLT\_RST# (pin 9), INT\_SERIRQ (pin 11), PWRSW# (pin 13), +5VRUN (pin 15), +ECVCC (pin 17), E51RXD (pin 19), E51TXD (pin 21), SB\_RST# (pin 23), LPC\_AD0 (pin 31), LPC\_AD2 (pin 33), LPC\_FRAME# (pin 34), ID\_LPC\_PCI# (pin 35), PM\_CLKRUN# (pin 36), PCLK\_FWH (pin 37), PCLK\_FWH (pin 38), PCI\_RST# (pin 39), and 30MIL TP588 (pin 40).

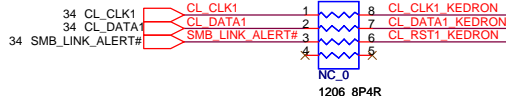
Pinout diagram for the X-BUS connector. The diagram shows a 40-pin connector with pins numbered 1 to 40. Pins 1-19 are labeled XIO FA0 to XIO FA19. Pins 20-24 are labeled MEMCS#, FRD#, FWR#, CARD\_INSERT, and EC\_OUT1. Pins 25-39 are labeled XIO FD0 to XIO FD19. Pins 40-44 are labeled XIO FD20 to XIO FD24. The diagram also shows connections to +ECVCC, C806 0.1U\_16V\_Y, 0402\_Y5V, and ground.



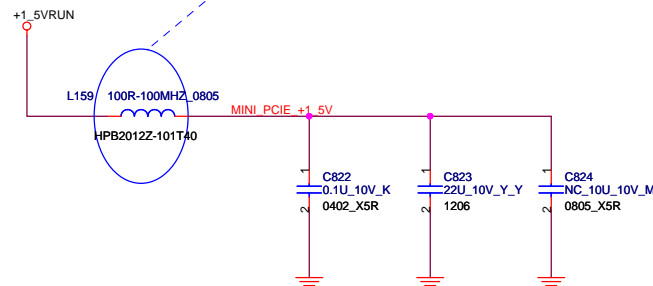
## WLAN Switch



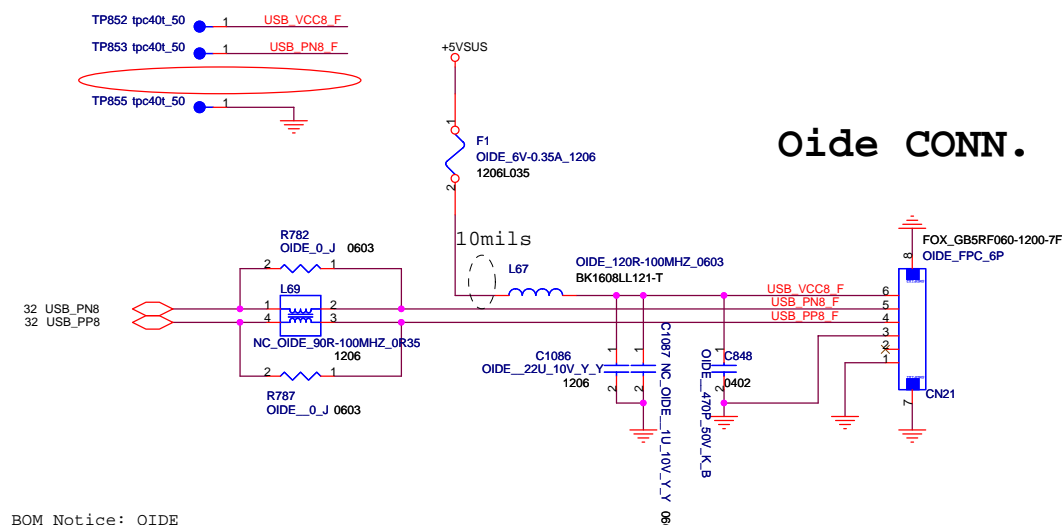
## Mini Card. WLAN



For EMI.

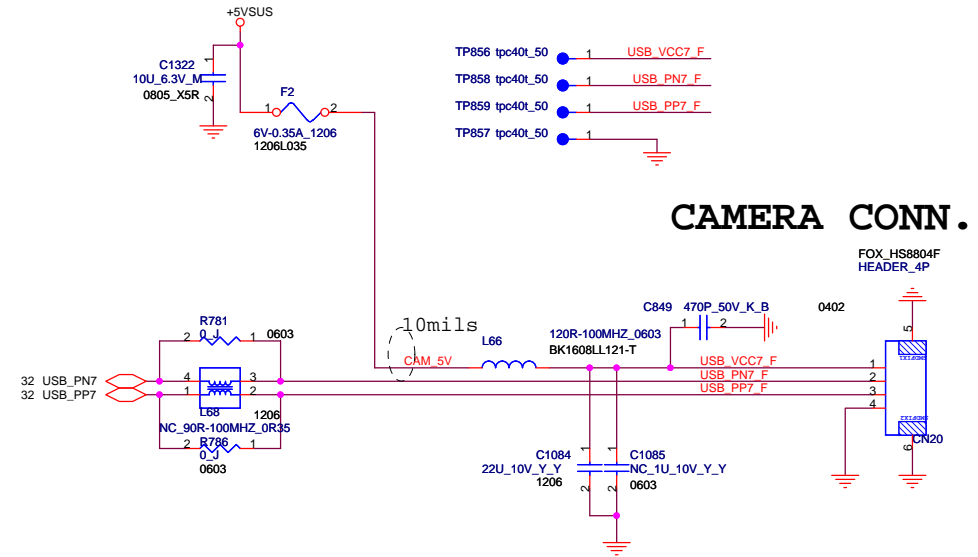


FOXCONN			HON HAI Precision Ind. Co., Ltd.
Mini-PCIE Card			CCPBG - R&D Division
Size	Document Number	Rev	
A3	MS91-1-01	1.0	
Date:	Thursday, June 21, 2007	Sheet	40 of 66

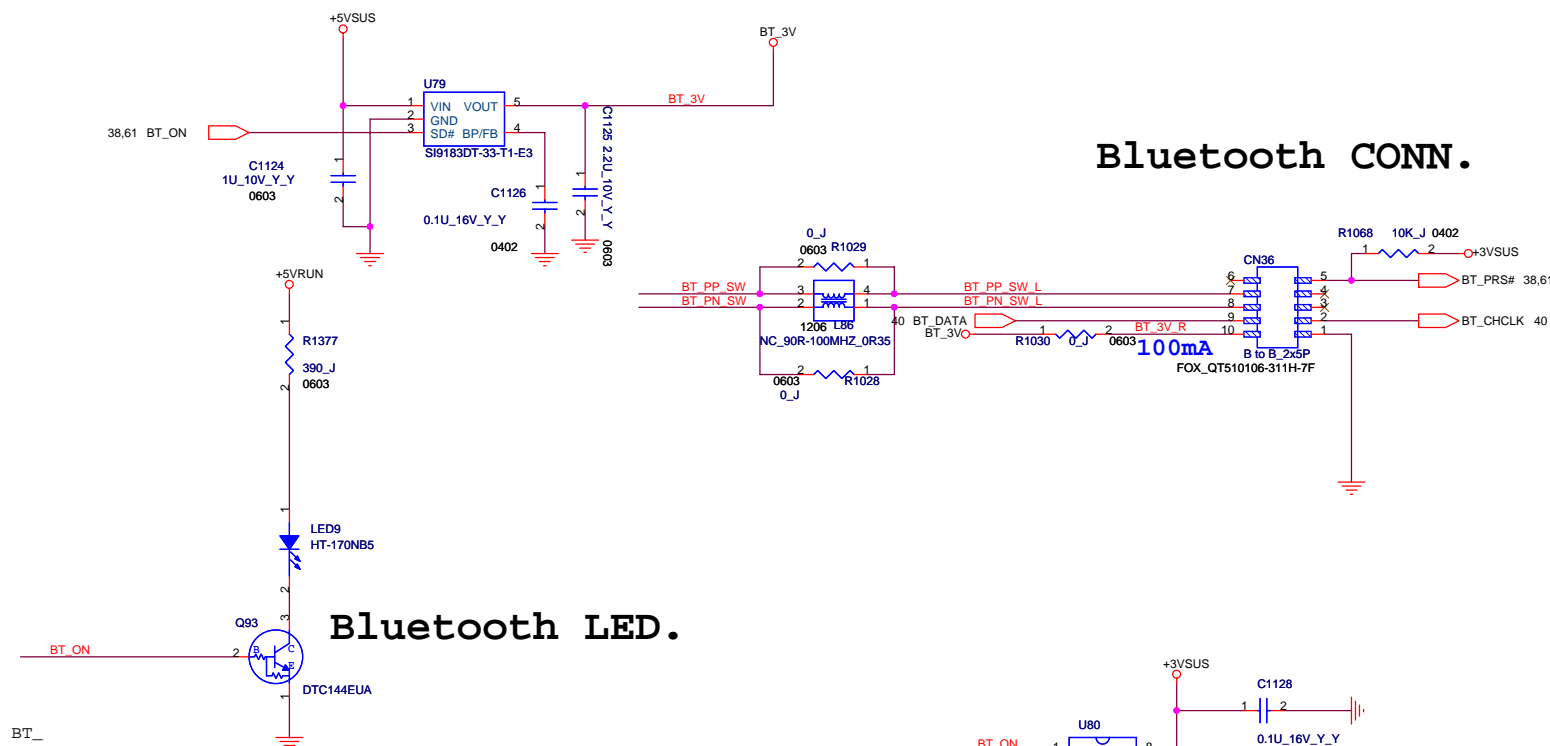


BOM Notice: OIDE\_

W/ Oide SKU	R782,R787,L67,C1086,C1087,C848,CN21	stuff
W/O Oide SKU	R782,R787,L67,C1086,C1087,C848,CN21	no stuff



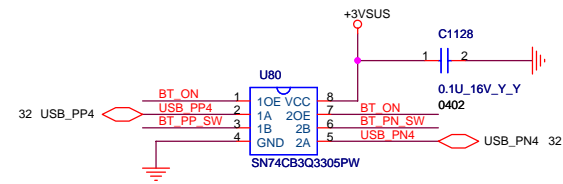
## Bluetooth CONN.



## Bluetooth LED.

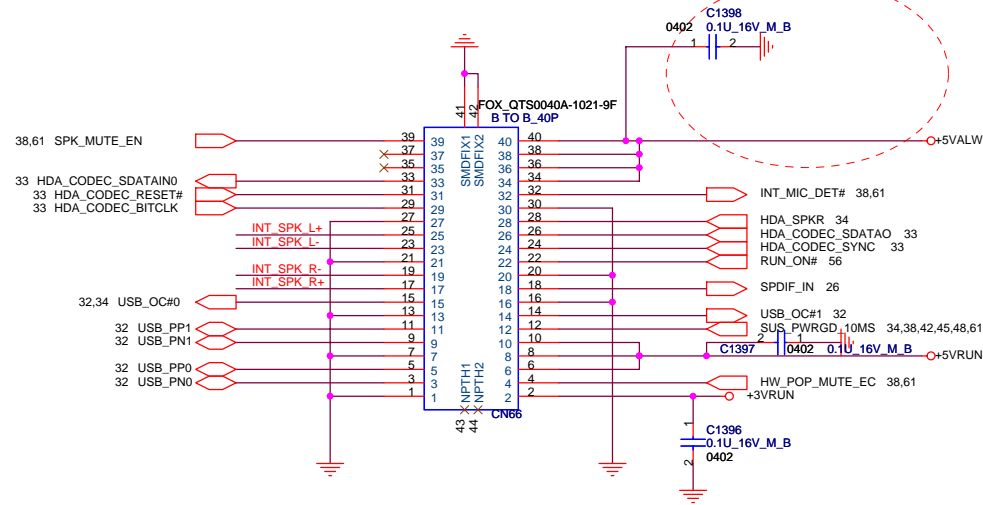
BOM Notice: BT\_

W/ BT SKU	Q93,LEDE9,R1377,U79,C1124,C1125,C1126,C1128,U80,R1068,R1028,R1029,R1030,CN36	stuff
W/O BT SKU	Q93,LEDE9,R1377,U79,C1124,C1125,C1126,C1128,U80,R1068,R1028,R1029,R1030,CN36	no stuff

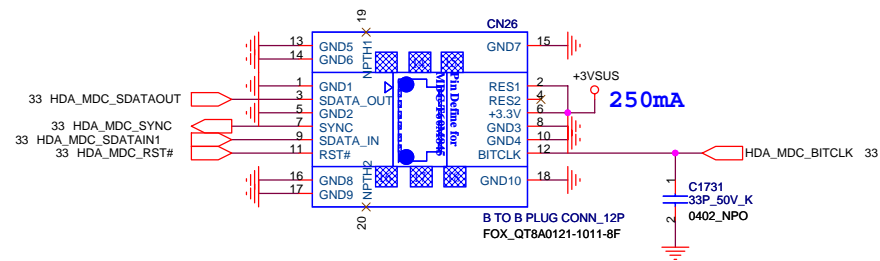




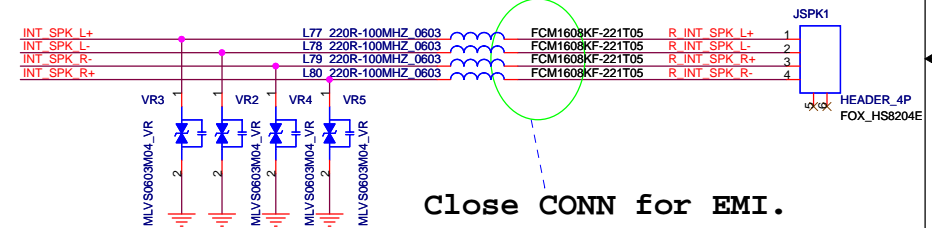
## Audio & USB Board CONN.



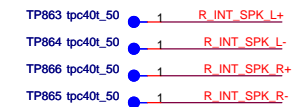
**MDC CONN.**



## INTERNAL SPEAKER

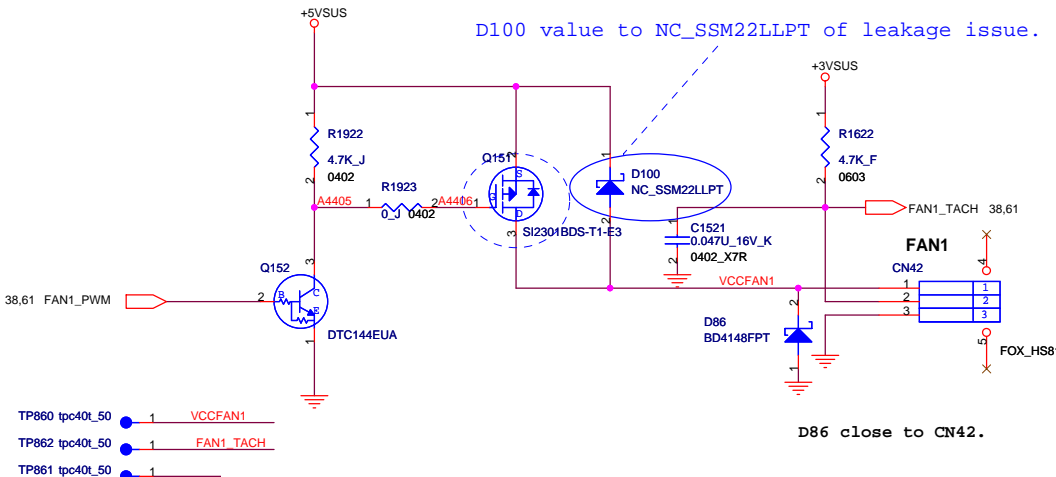


Close CONN for EMI.



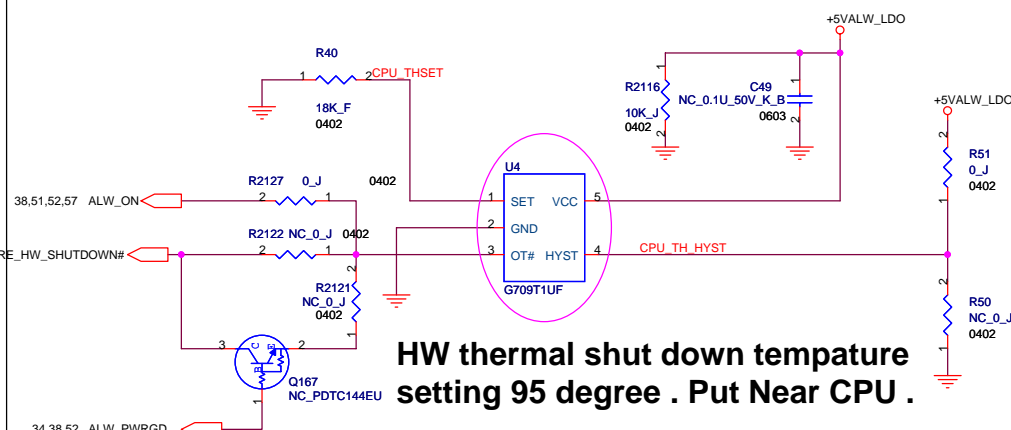
0331: Add diode for inverse current and change pull-high resistor from 10K to 4.7K.

0331: Change C1521 from Y5V to X7R.



FAN

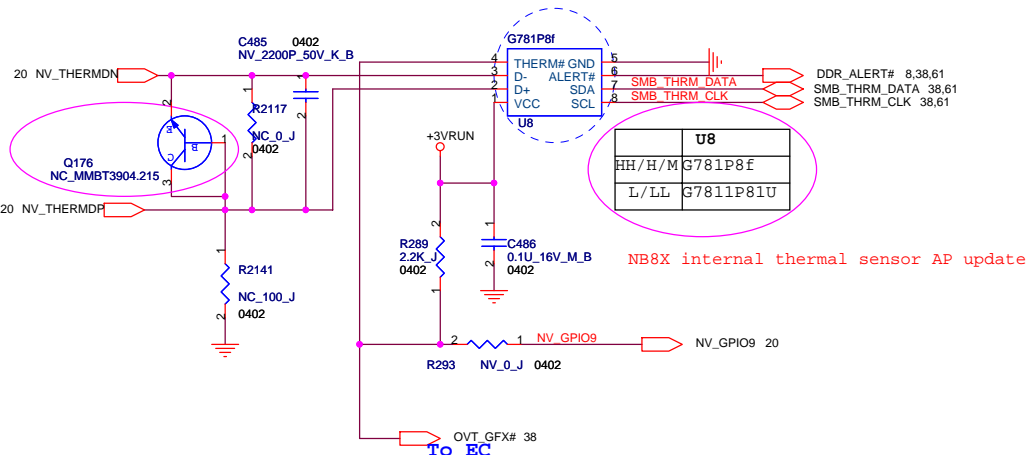
HW THERMAL PROTECTION



Delete VGA Thermal-Sensor

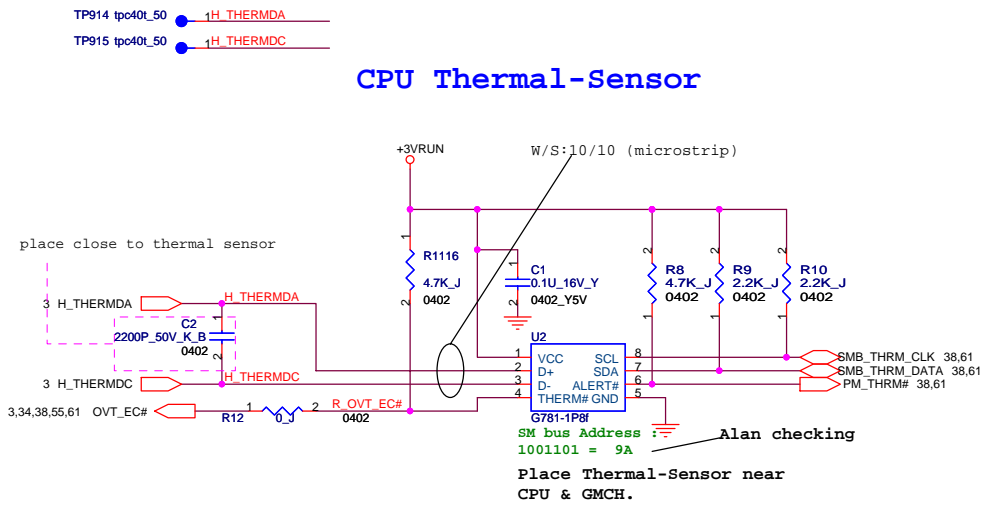
Delete local DDR2 themarl sensor.

SM bus Address :  
1001100 (EC)  
For G781P8f

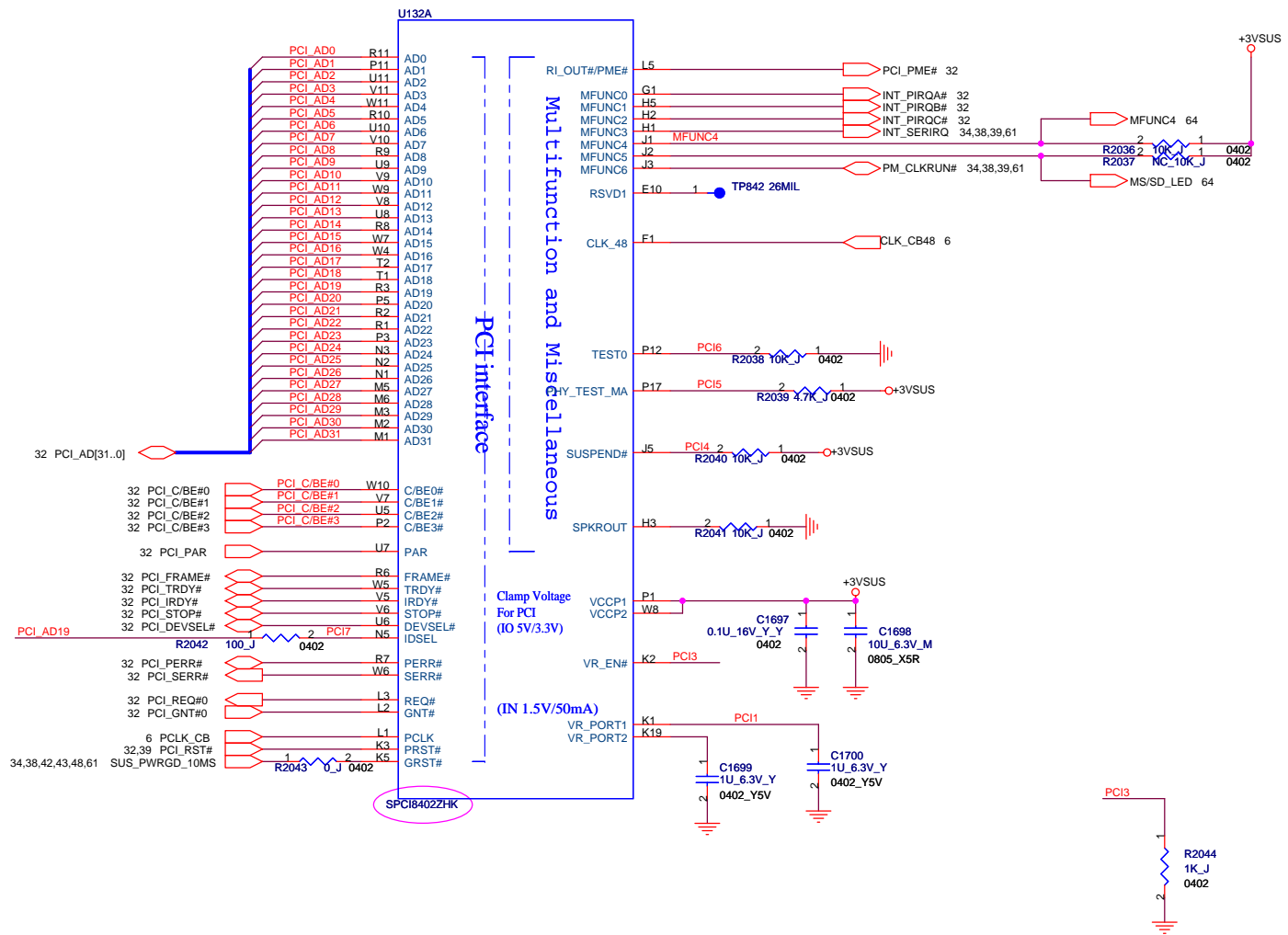


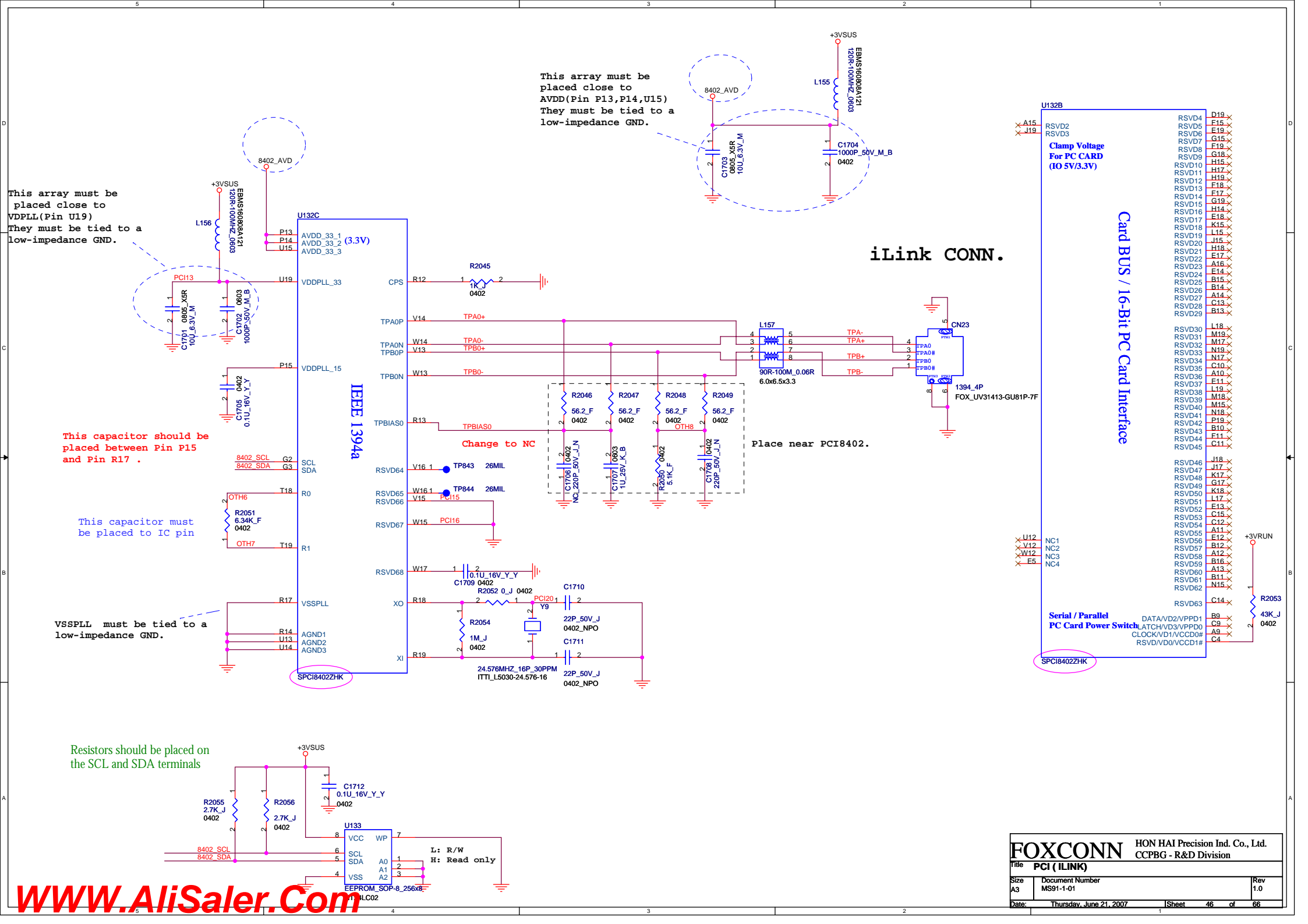
Close to U7

CPU Thermal-Sensor

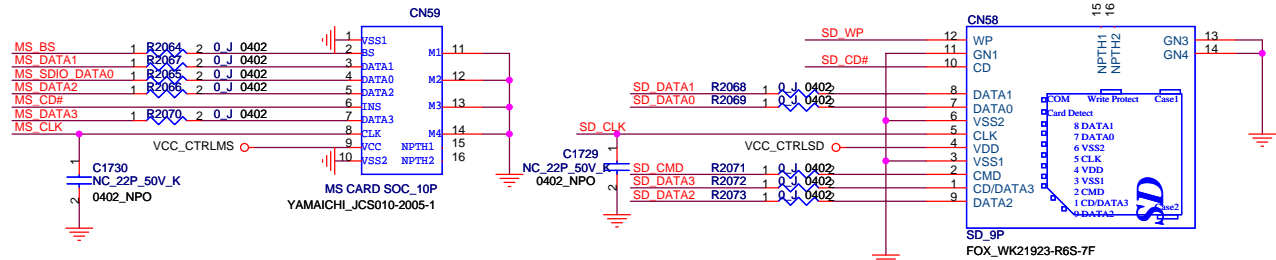
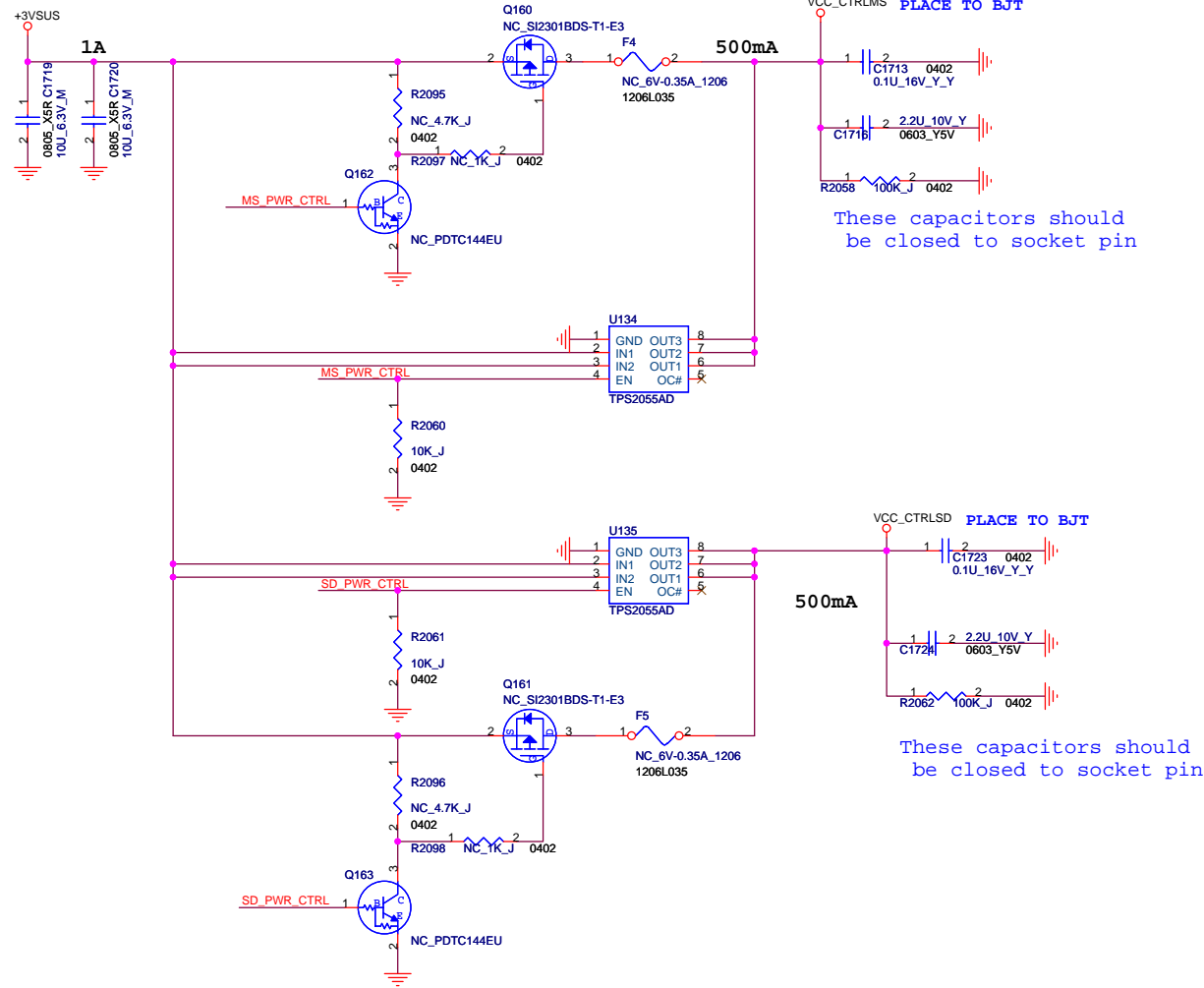
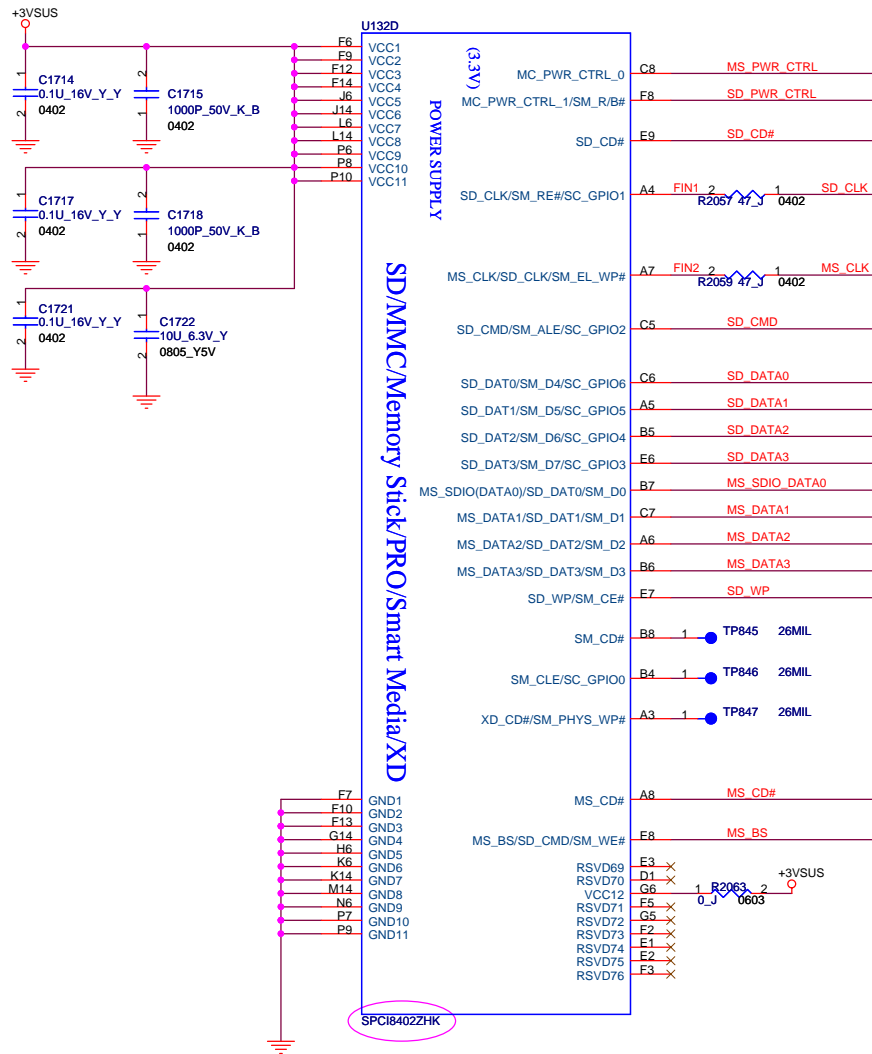


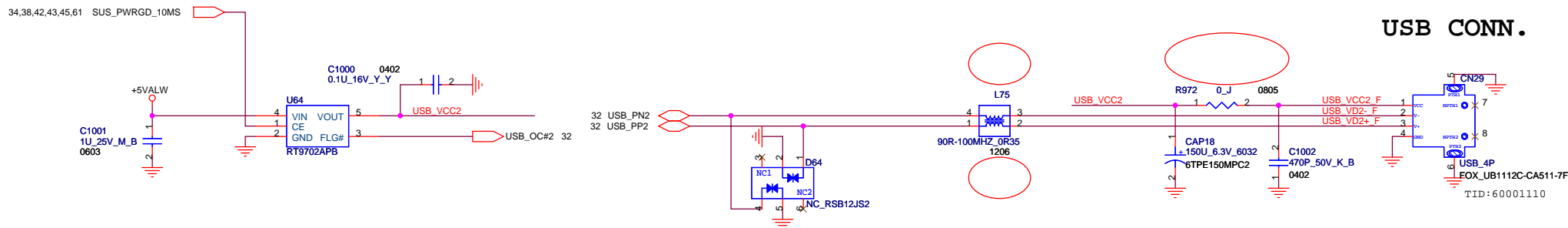
Close to U109

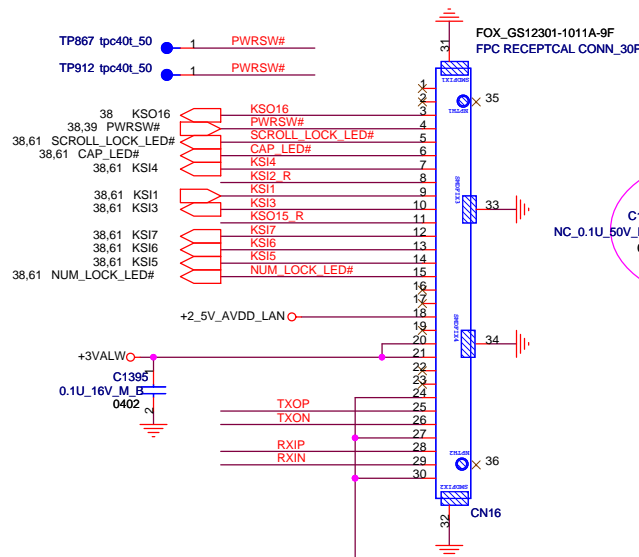




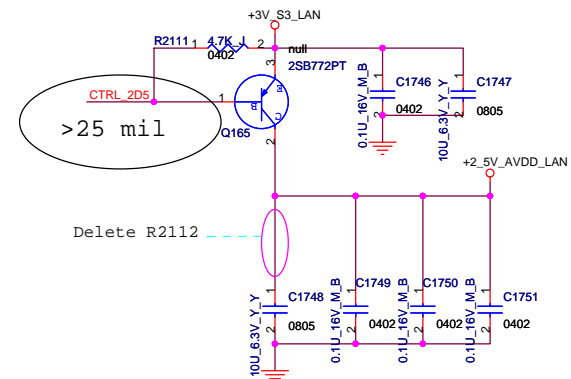
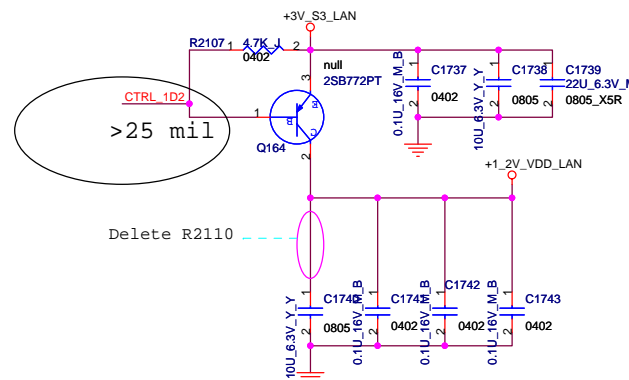
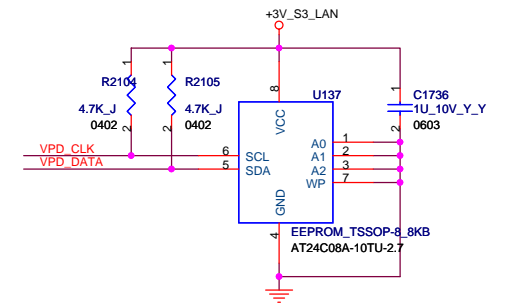
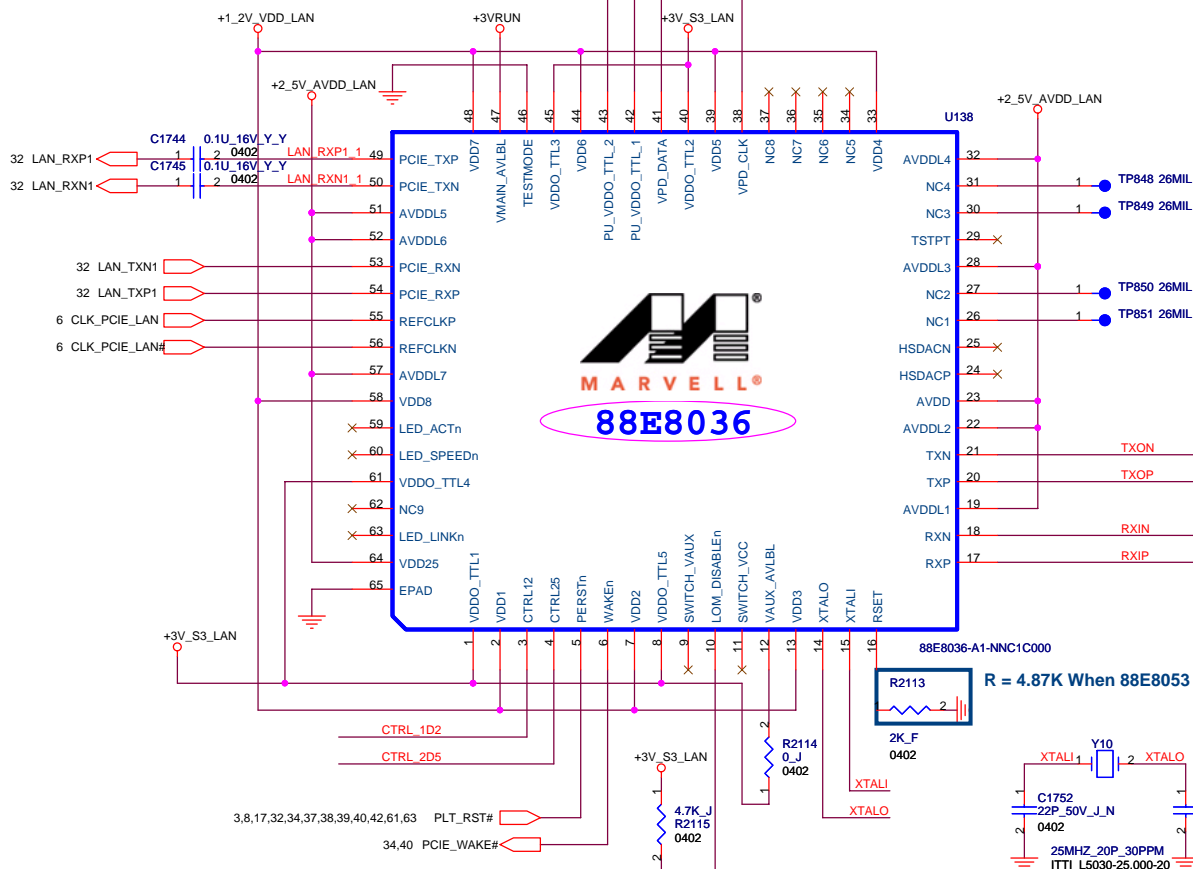




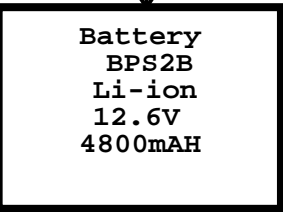
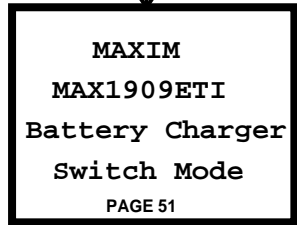
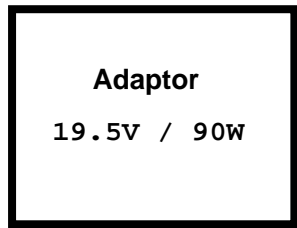




## Switch Board CONN.

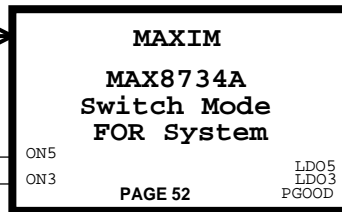


FOXCONN HON HAI PRECISION IND. CO., LTD.		
CPBG - R&D Division		
Title	<b>LAN (88E8039)</b>	
Size	Document Number	Rev
A3	MS91-1-01	1.0
Date:	Thursday, June 21, 2007	Sheet 49 of 66



DCBATOUT

ALW\_ON



System

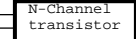
+5VALW/5A

System

+3VALW/5A

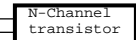
+5VALW\_LDO  
+ECVCC  
ALW\_PWRGD

SUS\_ON



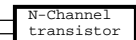
+5VSUS/1.6A

RUN\_ON



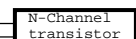
+5VRUN/3A

SUS\_ON



+3VSUS/1.6A

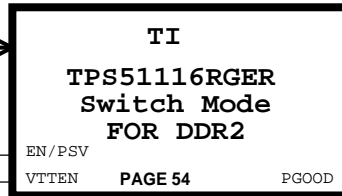
RUN\_ON



+3VRUN/3A

DCBATOUT

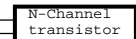
SUS\_ON



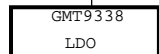
+1\_8VSUS/11A

+0\_9VSUS/2A  
DDRDIMM\_VREF  
DDR2\_PWRGD

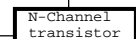
RUN\_ON2



+1\_8VRUN/6A



RUN\_ON

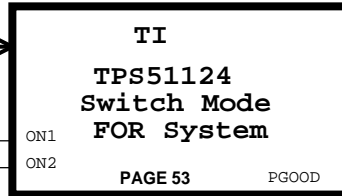


+1\_25RUN/1.7A

DCBATOUT

SUS\_ON

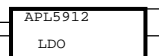
RUN\_ON



+1\_05VRUN/5A

+1\_5VRUN/6A  
RUN\_PWRGD

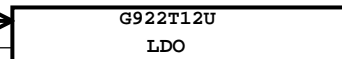
RUN\_ON1



PEX\_VDD/1.61A

DCBATOUT

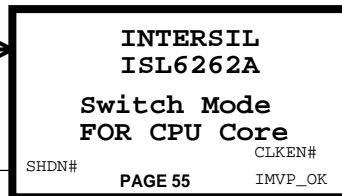
SUS\_ON



+8V For Load switch

DCBATOUT

IMVP\_VR\_ON

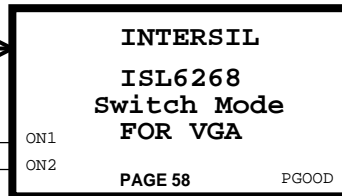


VHCORE/44A

EC\_CLK\_EN#  
IMVP\_OK

DCBATOUT

RUN\_ON1

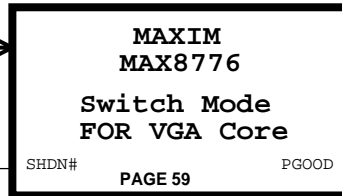


PEX\_VDD(1.2V)/1.61A

NV\_VDD(1.1V)/14.7A

DCBATOUT

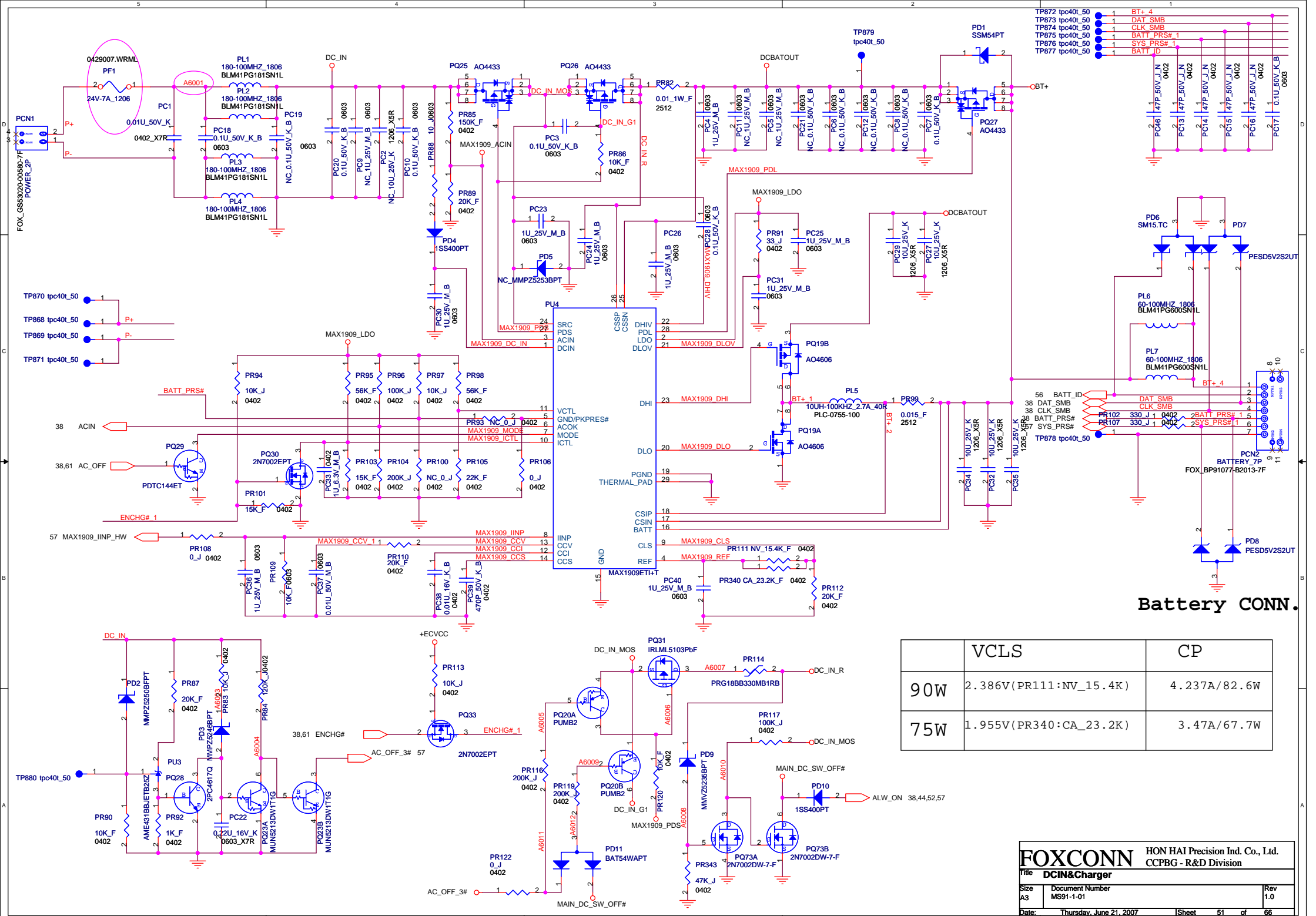
DFGT\_VR\_EN

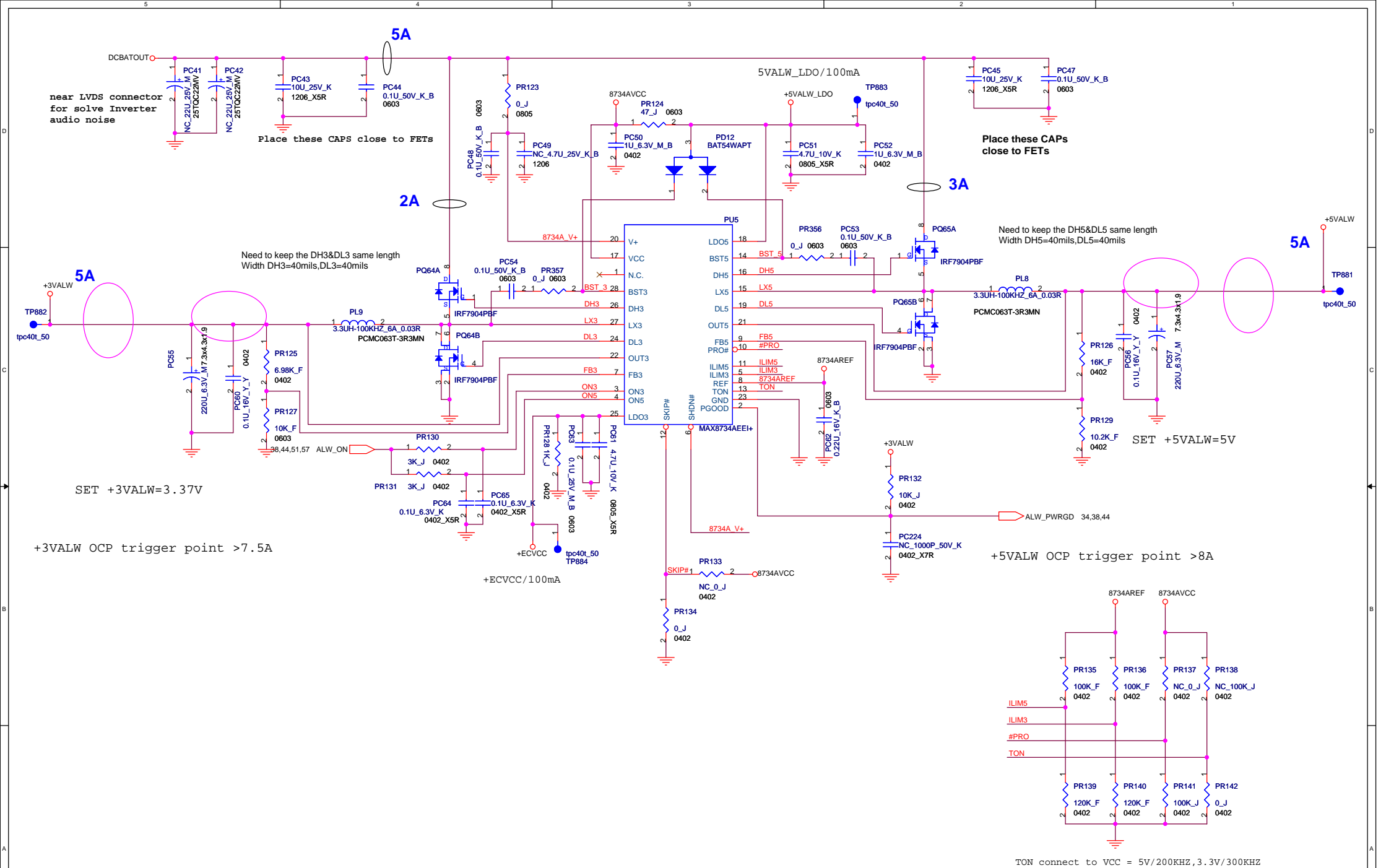


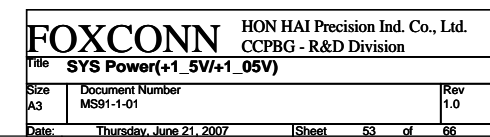
+VGFX\_CORE/7.7A

**FOXCONN** HON HAI Precision Ind. Co., Ltd.  
CCPBG - R&D Division

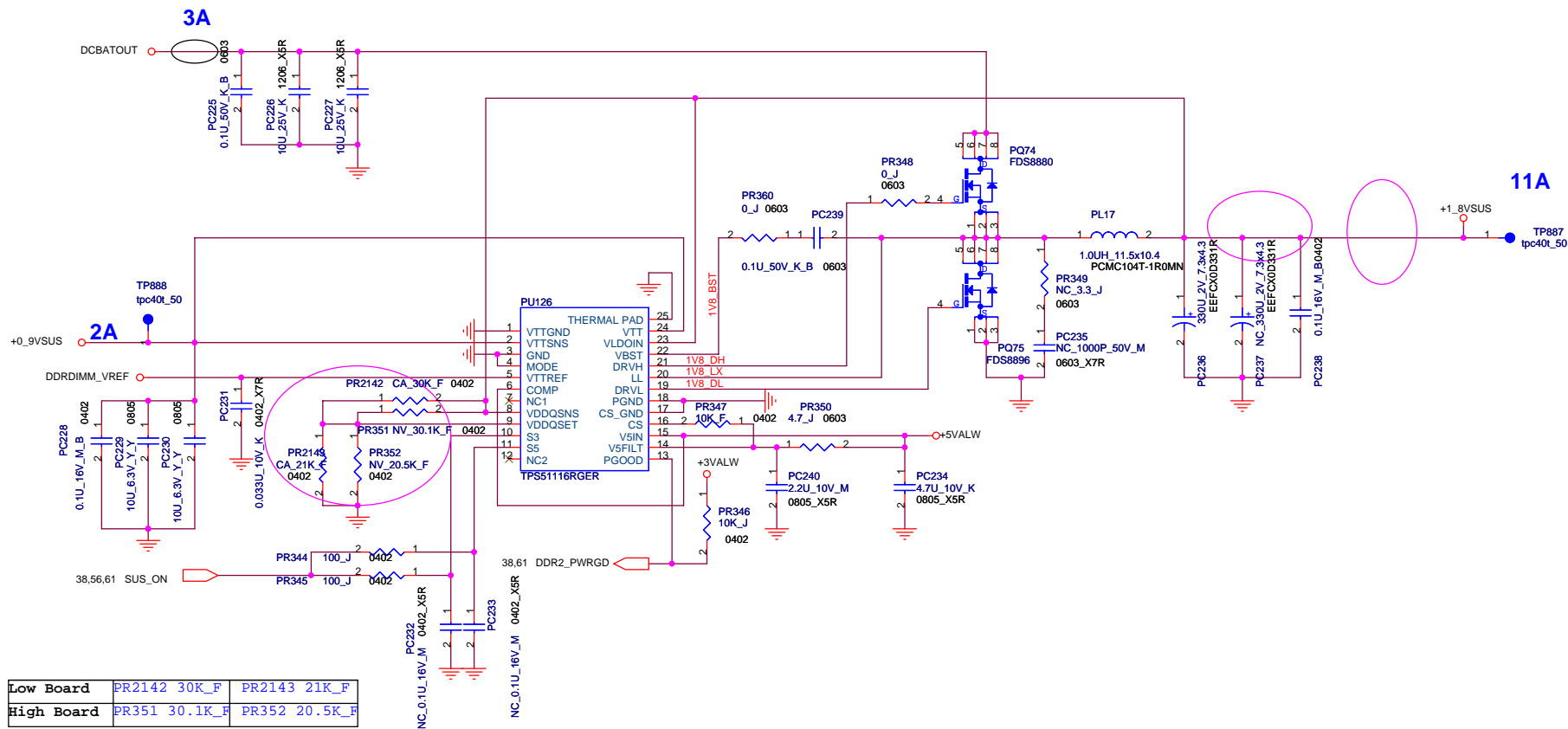
Title <b>Power Design Diagram</b>		
Size A3	Document Number MS91-1-01	Rev 1.0
Date: Thursday, June 21, 2007	Sheet 50	of 66



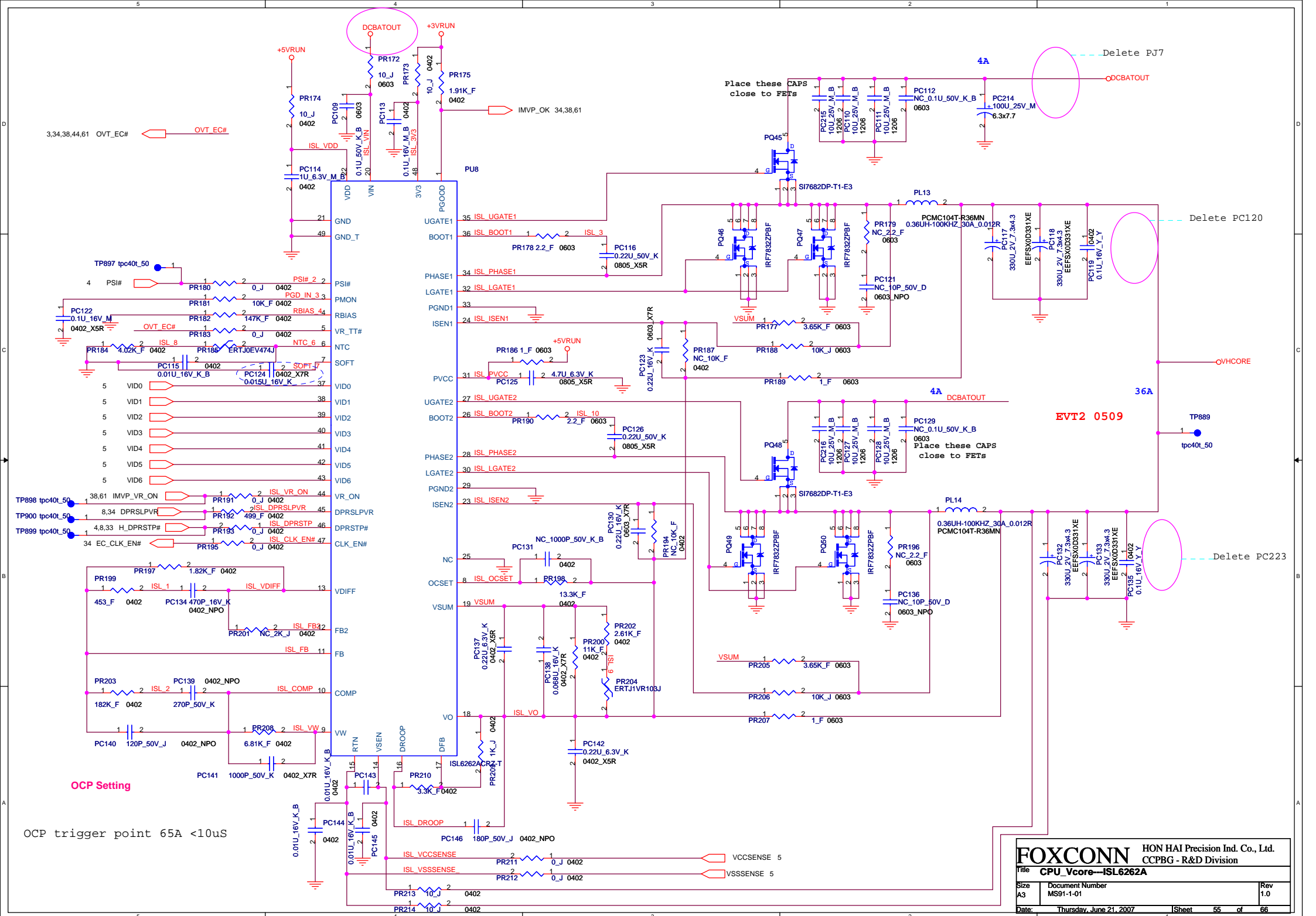




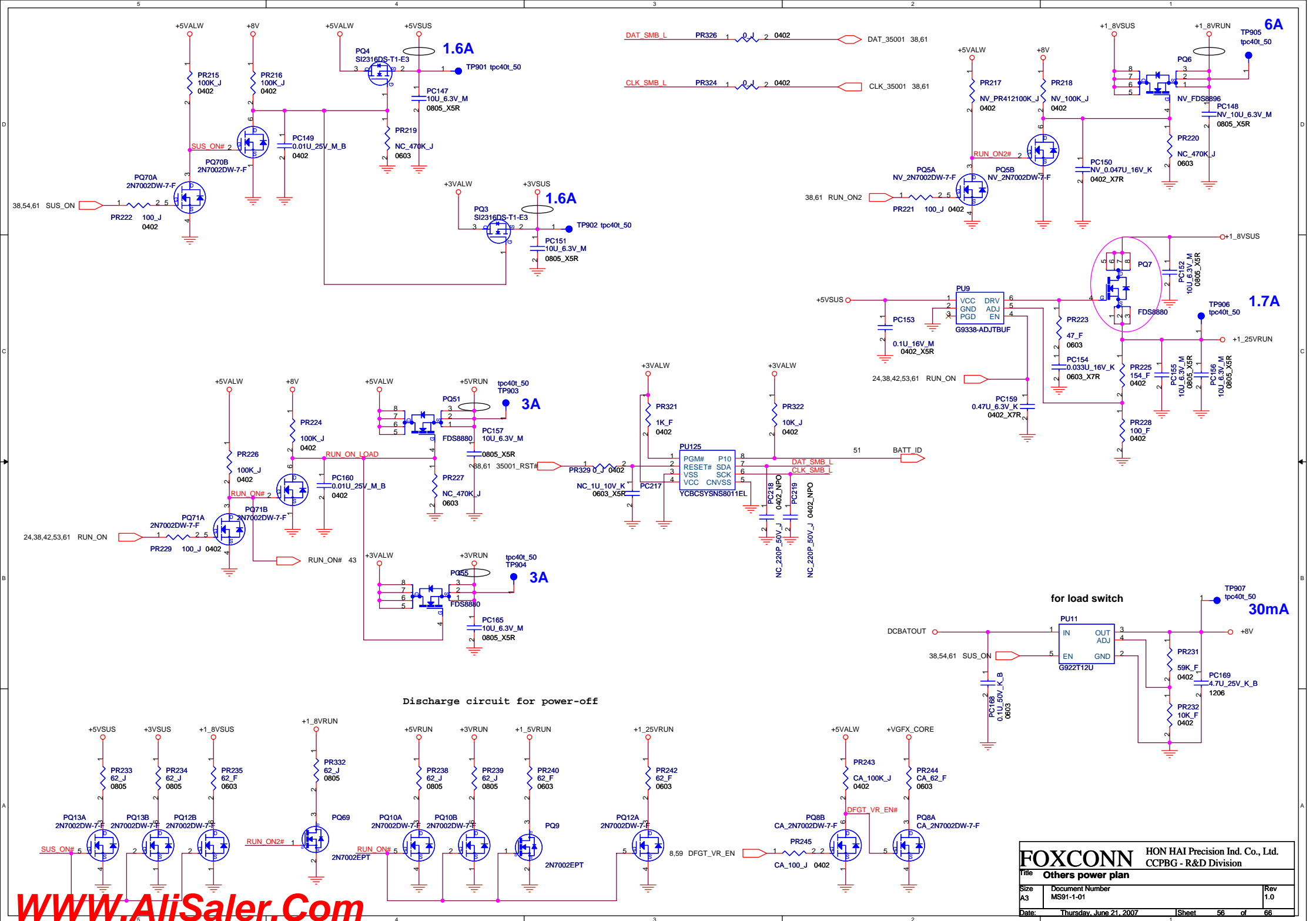


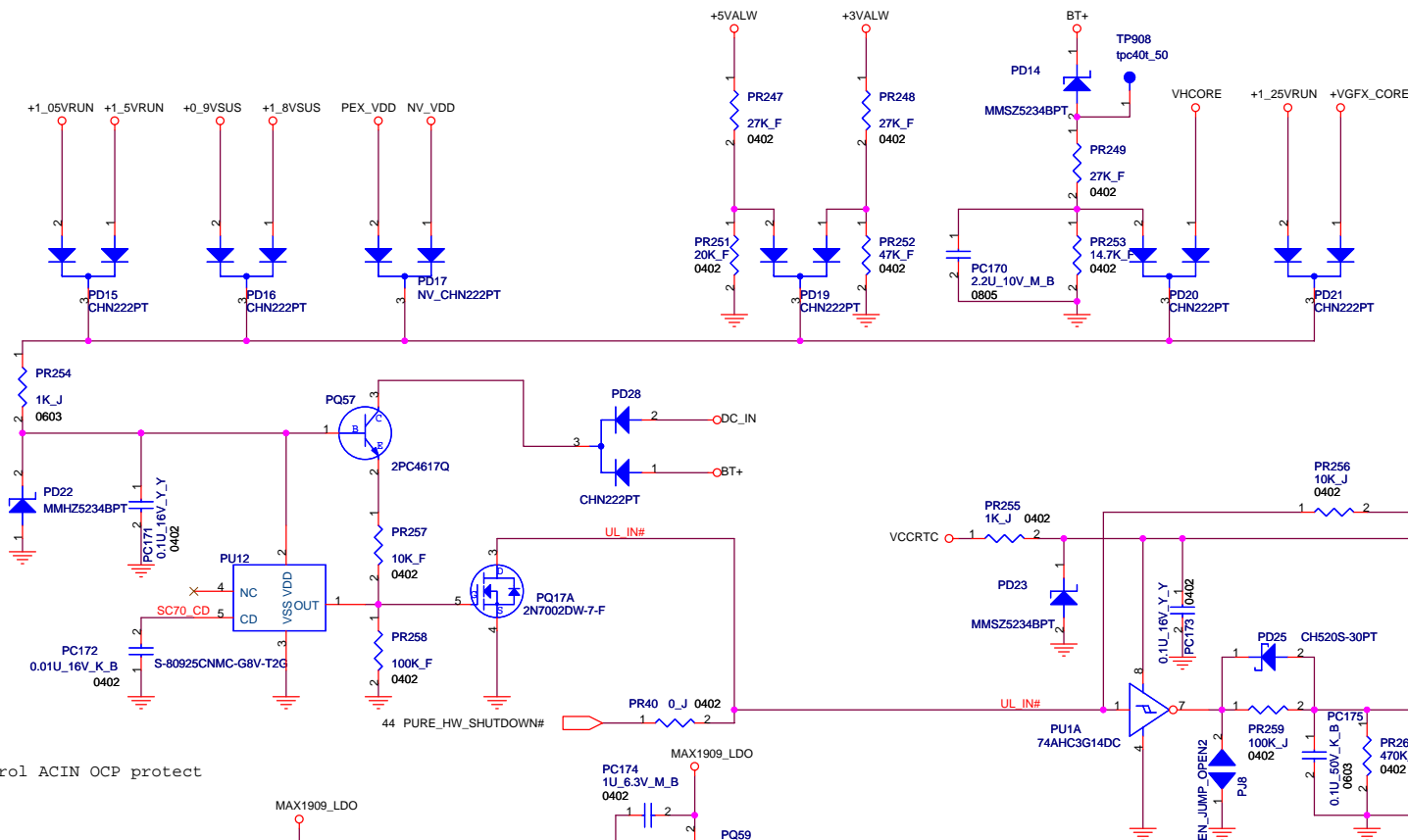


Setting +1\_8VSUS OCP trigger point to 16A

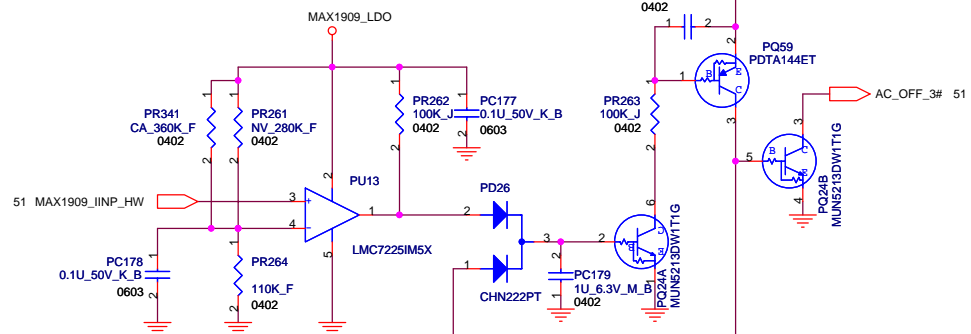


OCP trigger point 65A <10uS



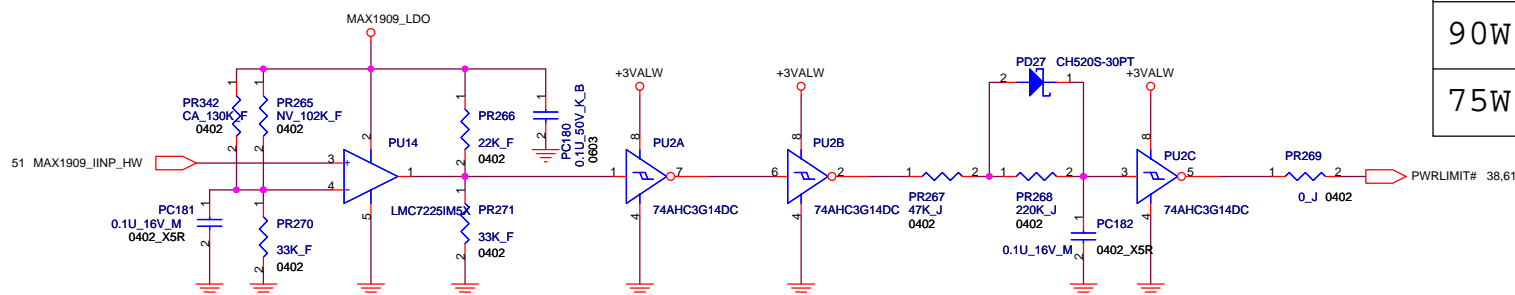


Control ACIN OCP protect



		ACIN OCP
90W	PR261:NV_280K	5.07A/98.9W
75W	PR341:CA_360K	4.21A/82.1W

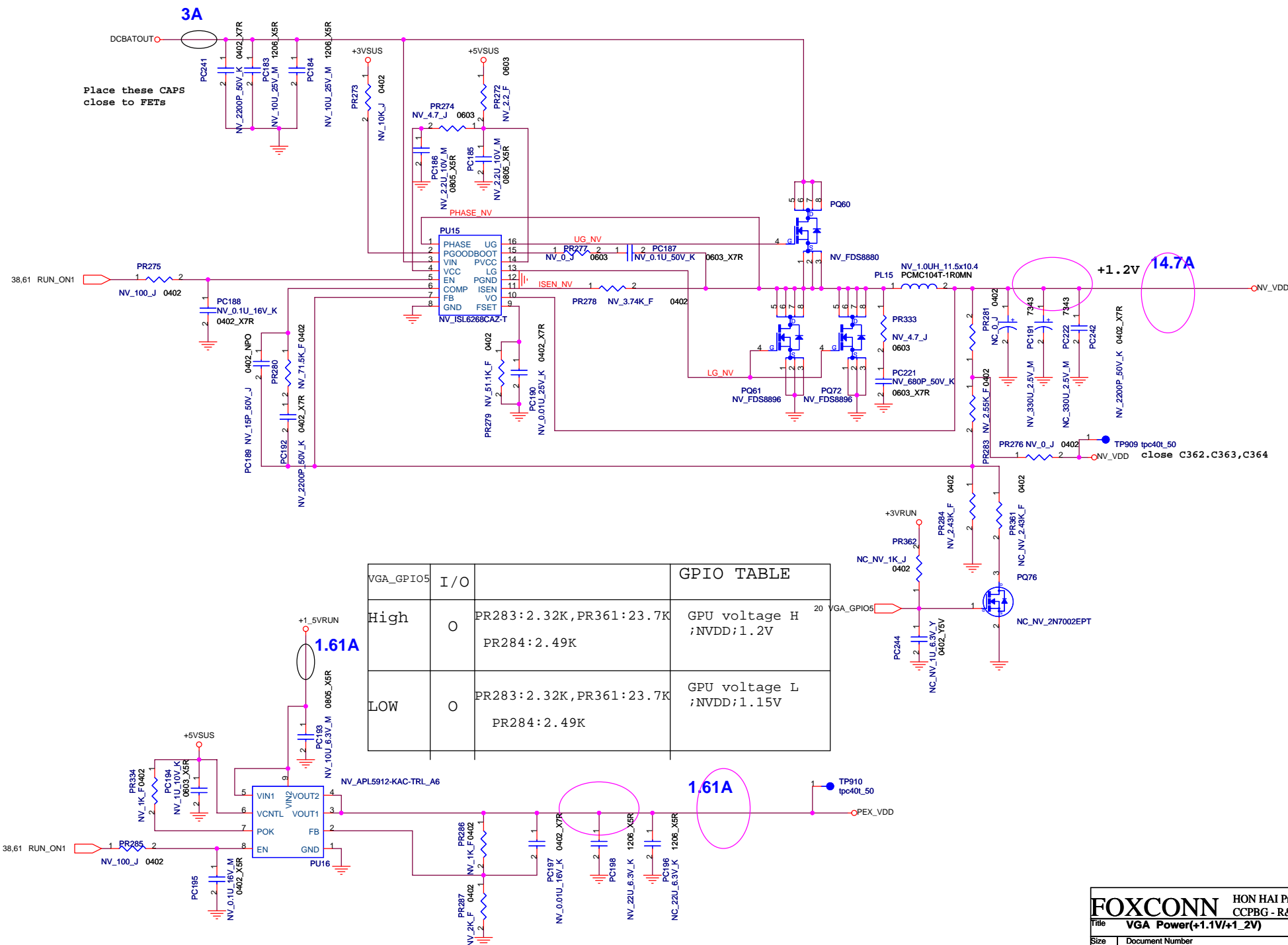
Setting ACIN OCP trigger point to 5.077A

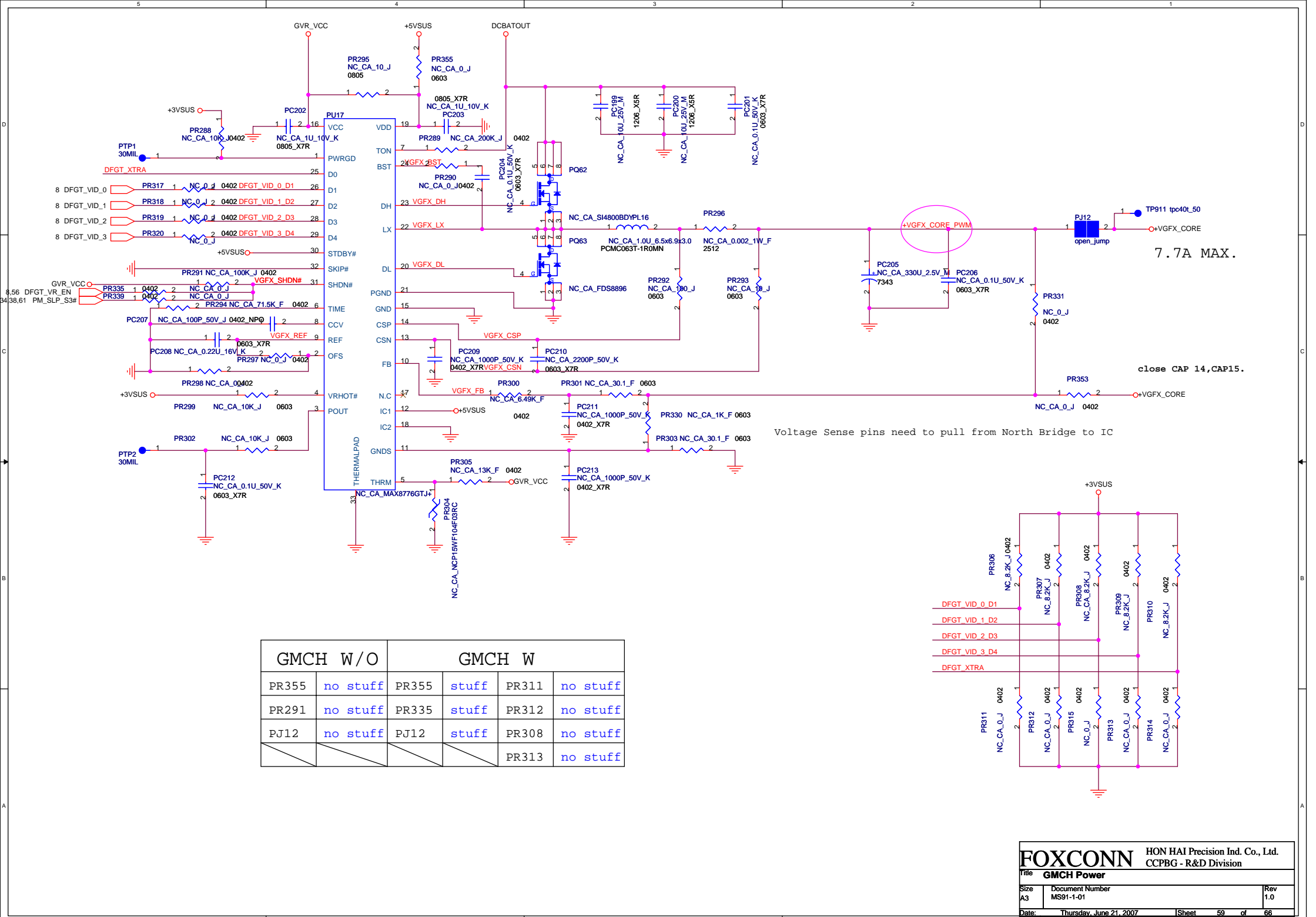


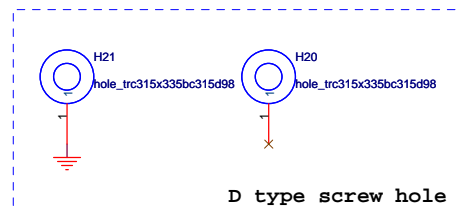
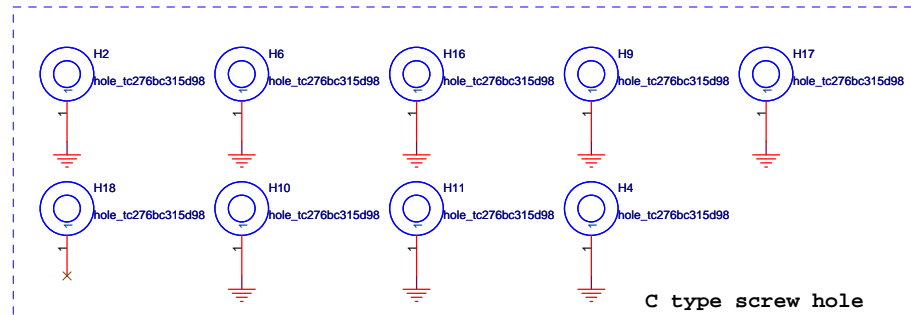
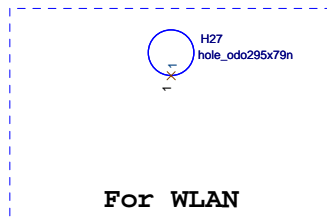
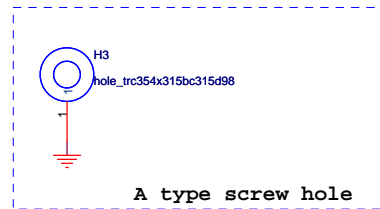
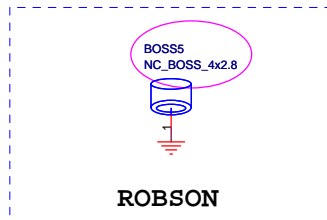
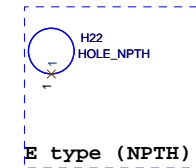
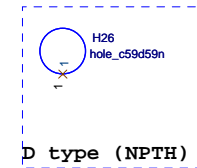
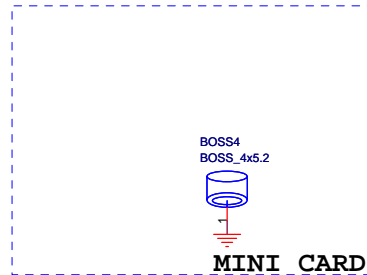
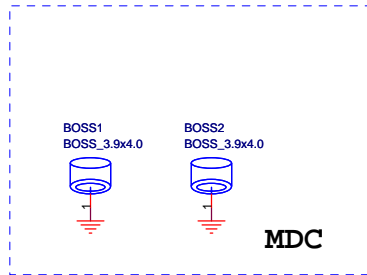
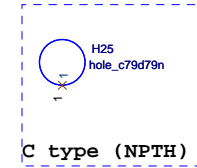
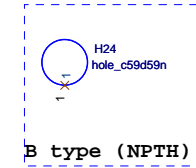
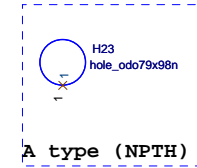
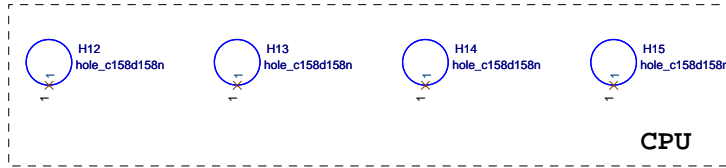
Setting PWRLIMIT# trigger point to 4.15A

		PWRLIMIT
90W	PR265:NV_102K	4.4A/85.8W
75W	PR342:CA_130K	3.64A/71W

+VGA\_CORE Ilimit =22.8A~27.38A

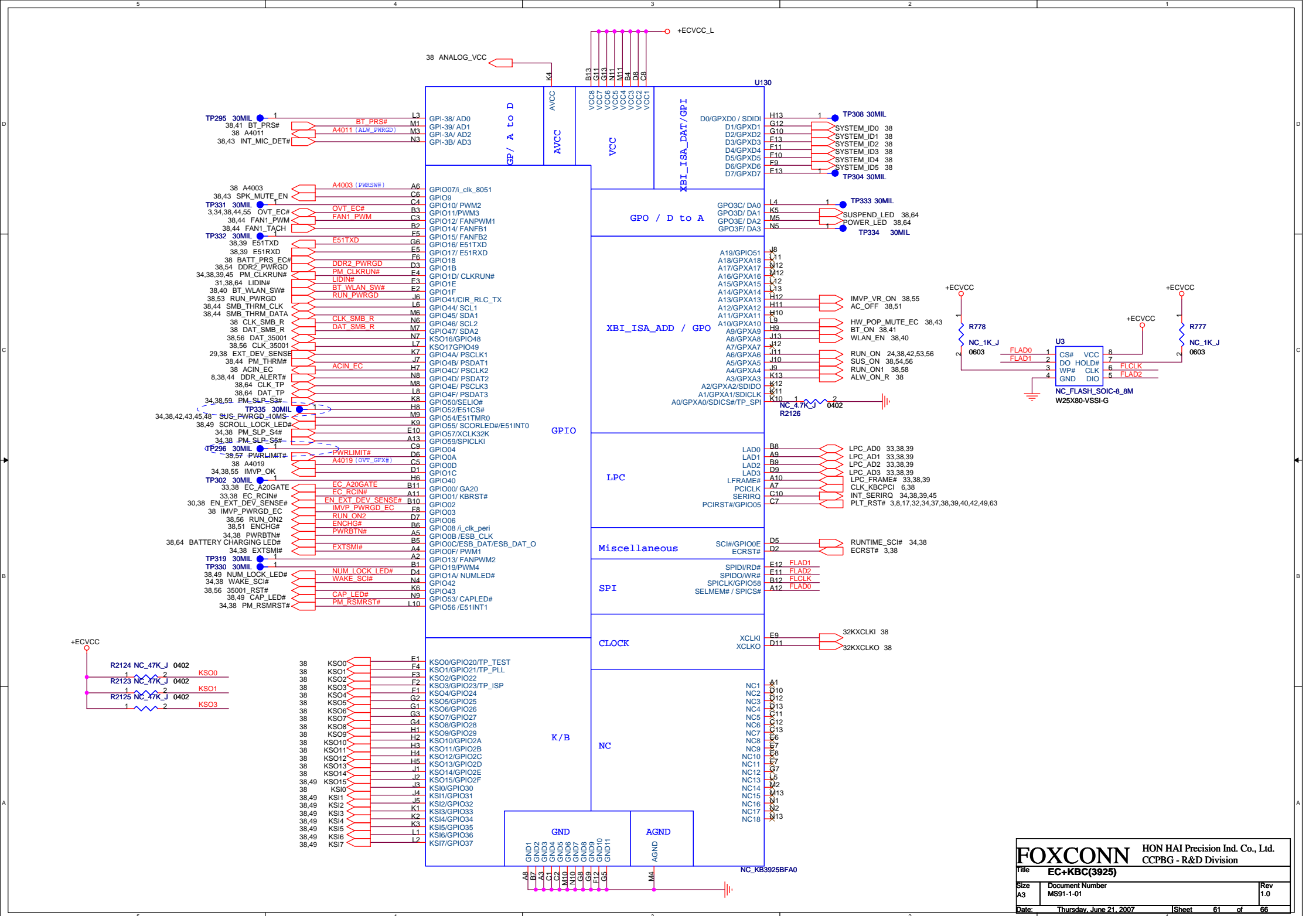






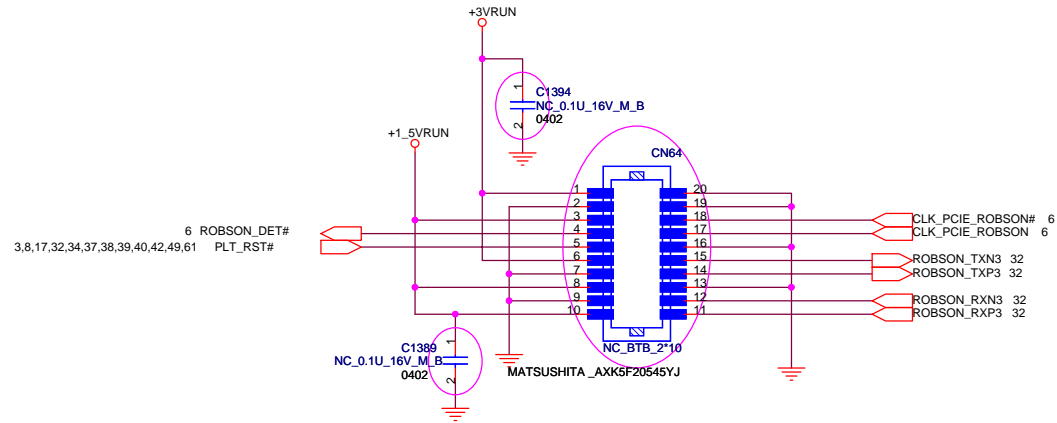
<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.
Title <b>HOLE</b>		CCPBG - R&D Division
Size A3	Document Number MS91-1-01	Rev 1.0
Date: Thursday, June 21, 2007	Sheet 60 of 66	



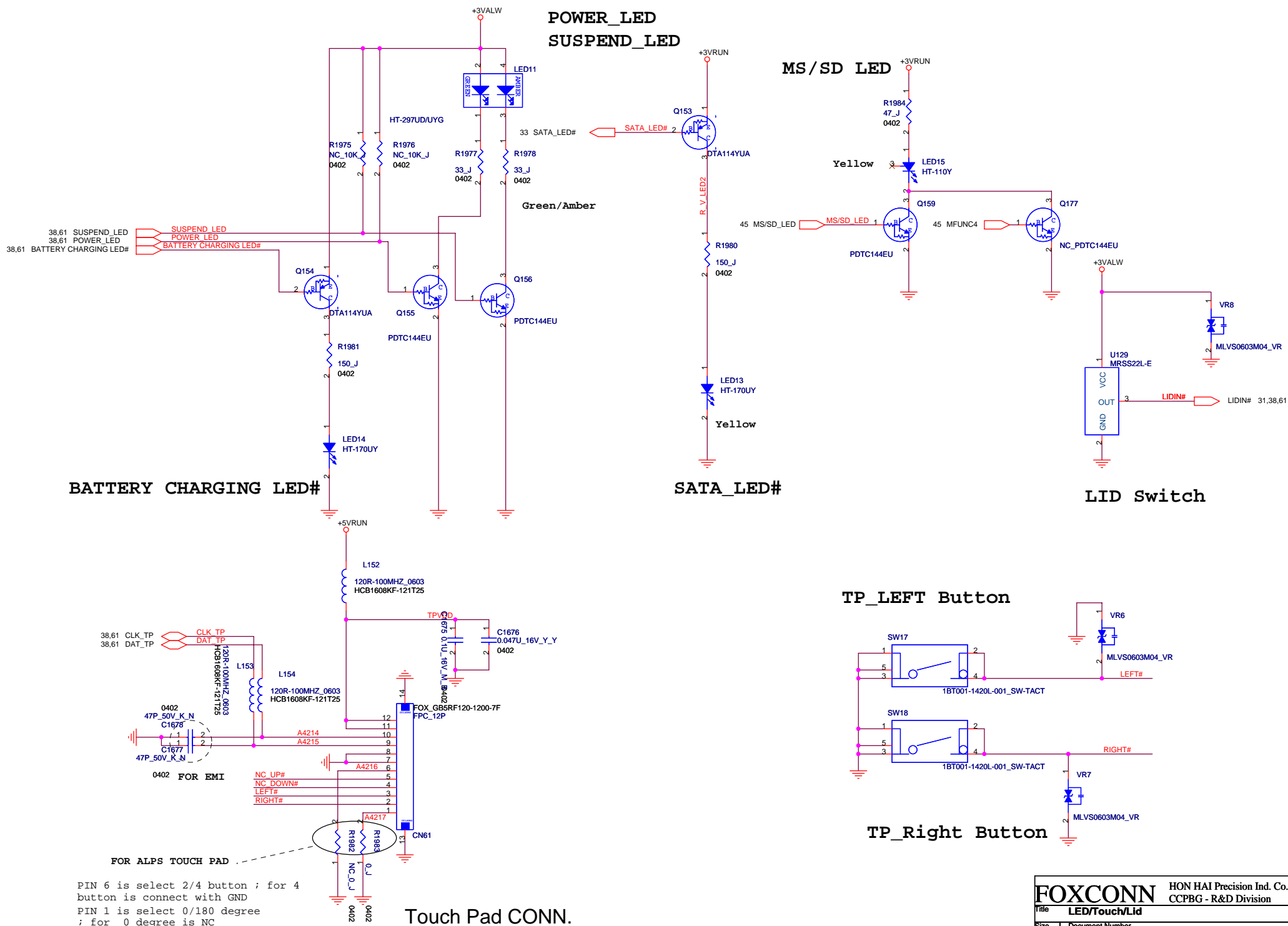




# ROBSON Board CONN



C1389,C1394 close to CN64.



MS91 DVT

(2007/04/04)

P.51 Move PF1 close to the PCN1 for MS1X burn out issue.

P.52,53,54,55,58 Add PJ1,PJ2,PJ3,PJ4,PJ5,PJ9,PJ11 for DVT debug.

P.54 Add PR2142, PR2143, change PR352 value 20.5K\_F to NV\_20.5K\_F, PR351 value 30.1K\_F to NV\_30.1K\_F.Because H version and L version need different voltage level.

P.6,32,63 Change RP11 value NC\_33 to 33,  
C1394 value NC\_0.1U\_16V\_M\_B to 0.1U\_16V\_M\_B,  
C1389 value NC\_0.1U\_16V\_M\_B to 0.1U\_16V\_M\_B,  
C735 value NC\_0.1U\_16V\_M\_B to 0.1U\_16V\_M\_B,  
C730 value NC\_0.1U\_16V\_M\_B to 0.1U\_16V\_M\_B,  
CN64 value NC\_BT\_B\_2\*10 to BT\_B\_2\*10,  
for robson function need.

(2007/04/06)

p.2 Block diagram update for MS91 feature spec.

P.49 Change U138 from MARVELL 88E8036 to MARVELL 88E8039 for MS91 feature spec.

P.18 Add two Hynix type: 16Mx32 (128-bit) and 16Mx32 (64-bit) for backup solution.

P.18 Change PCI device ID: Change  
R231 value NV\_2K\_J to NVNB8M\_2K\_J,  
R232 value NC\_2K\_J to NVNB8P\_2K\_J,  
R233 value NC\_2K\_J to NVNB8P\_2K\_J,  
R234 value NV\_2K\_J to NVNB8M\_2K\_J.

(2007/04/09)

p.51 Move the net A6001 close to PF1 for moved PF1.

p.30 Change C666 10P\_50V\_J\_N to NC\_10P\_50V\_J\_N,  
C669 10P\_50V\_J\_N to NC\_10P\_50V\_J\_N,  
C671 10P\_50V\_J\_N to NC\_10P\_50V\_J\_N for EMI request.

p.30 Add C668,C670,C672 for EMI request.

p.31 Add R459 for nVidia suggest.

(2007/04/11)

p.49 Delete R2110,R2112 for Marvell suggest.

p.38 Change touch pad power from +5VSUS to +5VRUN for design mistake.

p.55 Delete PC120 PC223 for save layout space.

(2007/04/12)

P.1 Add MS91 BOM configuration.

P.60 Change BOSS5 value NC\_BOSS\_4x2.8 to BOSS\_4x2.8 for lock robson.

(2007/04/13)

P.52 Add net name +3VALW\_PWM and +5VALW\_PWM becuase add PJ2 and PJ1.

P.53 Add net name +1\_5VRUN\_PWM and +1\_05VRUN\_PWM becuase add PJ4 and PJ3.

P.54 Add net name +1\_8VSUS\_PWM becuase add PJ5.

P.55 Delete PJ7 and change DCBATOUT+ to DCBATOUT for save layout space.

P.58 Add net name NV\_VDD\_PWM and PEX\_VDD+ becuase add PJ9 and PJ11.

P.59 Add net name +VGFX\_CORE\_PWM becuase add PJ12.

(2007/04/16)

P.1 Dropped the NB8P-SE/128MB and NB8P-SE/64M for MOR request.

P.18 Delete two Hynix type: 16Mx32 (128-bit) and 16Mx32 (64-bit) for needless to backup solution.

(2007/04/17)

P.44 Add U8 solution for H/L has differente thermal sensor.

Change Q176 value from CA\_MMBT3904.215 to NC\_MMBT3904.215 for new solution.

P.44 Delete C62,U139,R2031,R2032,R73 for delete VGA thermal sensor.

P.24 Change MIOB\_VDD current from 900mA to 10mA.  
NV\_DACA\_VDD from 135mA to 130mA.  
NV\_DACB\_VDD from 200mA to 130mA.  
NV\_PLLVDD from 60mA to 35mA+35mA.  
IFP\_CDIOVDD from 150mA+150mA to 50mA+50mA.  
IFPCD\_PLLVDD from 35mA to 75mA.  
IFP\_ABIOVDD from 130mA+130mA to 45mA+45mA.  
IFPAB\_PLLVDD from 35mA to 75mA for power budget spec.

P.25 P.26 Change FBA\_PLLAVDD from 30mA to 15mA.  
FBC\_PLLAVDD from 30mA to 15mA.  
Change NB8M-GT xx mA to NB8X 1.5A.  
PEX\_PLL\_AVDD from 100mA to 75mA.  
PEX\_PLL\_DVDD from 20mA to 10mA.  
VDD33 from 110mA to 50mA.  
NV\_VDD from 16.25A to 13.37A.  
change NB8M-GT : 1.1V(TBD) to NB8X : 1.2V for power budget spec.  
Add H\_PLLVDD power budget spec 15mA.

P.27,P.28 Add +1\_8VRUN power budget spec 1.125A.  
change +1\_8VRUN from 1.2A to 1.125A for power budget spec.  
P.1 Update the PCB P/N.

(2007/04/17)

P.17,P.19,P.20,P.21,P.22,P.23,P.24,P.25,P.26 Change U7A,U7D,U7E,U7F,U7H,U7G,U7C,U7I value from NB8M-GT-B-A2/H to NV\_NB8M-GT-B-A2/H.

P.20 Change U82 to NV\_ for low board needless it.

(2007/04/23)

P.56 PQ7 Change from SI4800BDY to FDS8880 because the +1\_25VRUN load increase.

P.33 Add TP287 for test the RTCRST#.

P.49 Add C1559,TP288 for stable AV mode start.

(2007/04/24)

P.38 Change R715 to NV\_ for low board needless it.

(2007/04/24)

P.44 Change U4 from MAX6509HAUK-T+ to G709T1UF for PUR request.

(2007/04/27)

P.44,45,46 Change U132 from 12-PC18402-0000 to 12-SPC1840-0000 for PUR suggest.

(2007/05/07)

P.11 Change D6,R4 from CA\_ to stuff all the SKU for Intel suggest.

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	<b>History ( 1 )</b>		
Size	Document Number	Rev	
A3	MS91-1-01	1.0	
Date:	Thursday, June 21, 2007	Sheet	65 of 66

**MS91 PVT**  
**(2007/05/30)**  
P.43 Add Polyswitch (F7) and resistor (R2142)\_NC co-layout on USB power input of M/B for TUV  
P.48 Add Polyswitch (F8) and change resistor R972 from stuff to NC co-layout on USB power input of M/B for TUV

**(2007/06/01)**  
P.6,32,60,63 Change RP11 value 33 to NC\_33,  
C1394 value 0.1U\_16V\_M\_B to NC\_0.1U\_16V\_M\_B,  
C1389 value 0.1U\_16V\_M\_B to NC\_0.1U\_16V\_M\_B,  
C735 value 0.1U\_16V\_M\_B to NC\_0.1U\_16V\_M\_B,  
C730 value 0.1U\_16V\_M\_B to NC\_0.1U\_16V\_M\_B,  
CN64 value BTB\_2\*10 to NC\_BTBTB\_2\*10,  
Change BOSS5 value BOSS\_4x2.8 to NC\_BOSS\_4x2.8 for lock robson.  
for robson function Disable.

**(2007/06/05)**  
P.52,53,54,55,58 Del PJ1,PJ2,PJ3,PJ4,PJ5,PJ9,PJ11 for PVT stage.  
P.52 Del net name +3VALW\_PWM and +5VALW\_PWM becuase del PJ2 and PJ1.  
P.53 Del net name +1\_5VRUN\_PWM and +1\_05VRUN\_PWM becuase del PJ4 and PJ3.  
P.54 Del net name +1\_8VSUS\_PWM becuase del PJ5.  
P.58 Del net name NV\_VDD\_PWM and PEX\_VDD+ becuase del PJ9 and PJ11.  
P.43 Change C1398 Pin 1 net name from +5VALW to +5V\_USB0\_1.  
P.48 Del co-layout resistor R971,R973 for level 6 suggest.  
P.41 Del TP854 for level 6 suggest.

**(2007/06/07)**  
P.43 Del Polyswitch (F7) and resistor (R2142)\_NC on USB power input of M/B for MOR suggest.  
P.48 Del Polyswitch (F8) and change resistor R972 from NC to stuff on USB power input of M/B for MOR suggest.

**(2007/06/08)**  
P.1,18 Add three BOM on BOM configuration for Hynix VRAM.  
P.38,49 Add option circuit for keyboard auto power on issue.  
1> Del TP294  
2> Add R2142(NC),R2143(NC),R2144(NC),R2145,R2146,R2147(NC).  
P.37 CN32 change from 2N-0050004-FKG0 to 2N-0050006-FKG0 for level 6 suggest.

**(2007/06/12)**  
P.24 Add R2148,R2149 for HDMI leakage issue.  
P.30 R/G/B add C1762(NC),C1763(NC),C1764(NC) for EMI suggest.

**(2007/06/20)**  
P.49 LAN controller U138 change from 88E8039 to 88E8036 for EMI fail issue.

<b>FOXCONN</b>		HON HAI Precision Ind. Co., Ltd.	
		CCPBG - R&D Division	
Title	<b>History ( 2 )</b>		
Size	Document Number	Rev	
A3	MS91-1-01	1.0	
Date:	Thursday, June 21, 2007	Sheet	66 of 66